INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDBU-2 STATIC BLINDER RELAY

* **CAUTION:** It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. Do not remove or insert printed circuit boards while the relay is energized. This may result in breaker tripping or component damage.

APPLICATION

The SDBU-2 relay provides the following functions in conjunction with the logic provided by the SRU relay:

1. Restricted trip function
2. Out-of-step blocking of tripping
3. Out-of-step blocking of reclosing
4. Out-of-step tripping

The SDBU-2 characteristic consists of two sets of two essentially parallel lines (actual arcs of extremely large circles) which form an angle with respect to the R-Axis on an R-X plot which is adjustable from 60° to 90°. The factory adjustment is 75°. Each set of parallel lines is equally spaced on each side of the origin of the R-X diagram. The relay has one output transistor per each set of the
* outside and inside set of parallel lines. Each output is negative when the relay is in the non-operate condition. It provides two outputs of 15.0 to 19.0 volts dc and up to 0.01 ampere of current when subjected to an ohmic value that falls inside each set of two characteristic lines.

The settings of the SDBU-2 relay define the ohmic reach from the origin in a direction perpendicular to the transmission line characteristics
* (Fig. 6).

CONSTRUCTION

The SDBU-2 relay consists of five air gap transformers (compensators), four center tapped auto-transformers, five phase shifting circuits, five isolating transformers, and several printed circuit assemblies.

Printed circuit boards are plug-in types which may be removed for tests or examination and then reinserted. They may also be plugged into a card extender, style #849A534G01, to make the test points and components accessible for in-service checking.

Compensator

The compensators which are designated I_{POL}, $+T_{AB1}$, $-T_{AB1}$, $+T_{AB2}$, and $-T_{AB2}$ are two winding air-gap transformers (Fig. 5). There are two primary current windings, each having seven taps which terminate at the tap block. They are marked 1.51, 2.00, 2.50, 3.50, 5.00, 7.1, and 10.0. I_{POL} compensator has no taps. A voltage is induced in the secondary which is proportional to the primary tap and current magnitude. This proportionality is established by the cross-sectional area of the laminated steel core, the length of the air gap which is located in the center of the coil, the tightness of the lamination. All of these elements have been precisely set at the factory. The clamps which hold the laminations should not be disturbed by either tightening or loosening the clamp screws.

* The secondary winding of the I_{OP} compensator
*is center-tapped to provide a voltage supply for the phase shifting network. The phase shifting network produces voltage in phase with the primary compensator current.

SUPERSEDES I.L. 41-489.2C
*Denotes change from superseded issue.

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Phase Shifting Circuits

Phase shifting of the input voltages is obtained through a circuit that consists of center-tapped autotransformers X_{A2}, X_{A3}, X_{A4}, X_{A5}, resistors P2 and capacitor C_{2A}, and resistor P3 and capa C_{3A}, resistor P4 and capacitor C_{4A}, resistor P5 and capacitor C_{5A} respectively.

In the current polarizing circuit the compensator voltage output is phase shifted by means of resistor R_{1A} and capacitor C_{A1}. The compensator voltage is supplied through the center tapped secondary of I_{POL} compensator.

Isolating Transformers

Transformers T1, T2, T3, T4, and T5 serve two purposes. First, they isolate the ac circuits from the dc circuit. Second, they amplify the clipped ac signal to make the relay sensitive to low level input signals.

Printed Circuit Board Assembly

The SDBU-2 relay uses six printed circuit boards (PCB) assemblies. The six PCB's are: one operating board, four polarizing boards; one is marked "+1", and one is marked "-1". These two boards refer to two inside characteristic lines of the relay. Further, one board is marked "+2" and one is marked "2". These two boards refer to two outside characteristic lines of the relay.

One "output board" contains two outputs. Output #1 (relay terminal #5) represents the inside characteristic and output #2 (relay terminal #6) represents the outside characteristic of the relay.

PCB assemblies shown in Figures 10 to 15 contain all the resistors, diodes, transistors, and thyristors necessary to perform the intended functions.

Components on each board are identified by a letter followed by a number so that every component has an exclusive identification. Resistors are identified by the letter R followed by a number. Similarly, diodes are identified by a D, and the cathode (the end out of which conventional current flows) is identified by a bar across the point of an arrow. Zener diodes are identified by Z, transistors by Q, thyristors by Qs, capacitors by C, and test points by TP.

Component letter designations are listed as below:

Capacitor C	
Diode D	Thyristor QS
Resistor R	Transistor Q
Test Point TP	Zener Diode Z (or DZ)

OPERATION

Four identical logic systems are used in the SDBU-2 relay. Each of the systems modifies the distance relay reach along the lines (T &U) as shown on Fig. 6. Two systems restrict the distance relays operation to the area left of T1 and T2 and two systems to area right of U1 & U2. Each of the systems presents a voltage to the static phase angle comparison unit which checks their phase angle relation to the operating voltage produced by I_{pol}. Each system voltage is composed of the phase shifted phase-to-phase voltage and the compensator output voltage that is proportional to the R component of the transmission line characteristic.

Complete operation of the relay is best illustrated by the set of phasor relations for selected conditions, as shown on Fig. 7. For simplicity assume relay characteristic is 90°, and operation of one unit only is considered.

Fig. 7 shows R-X diagram and several selected points Q, P, N, M, S located within the outside the operating area of the SDBU-2 relay designated by lines U and T. Depending on fault location currents are designated as I_p, I_q, I_m, I_n, or I_s.

Relay tripping conditions occur when the phasor designated V_{OP} leads phasor V_U and V_T simultaneously. Phasor $V_{OP} = KI_p$ is derived from the compensator designated "I_{POL}" and phase shifted by means of phase shifting circuit P1 and C1 to be in phase with the primary current I. Phasor V_U controls the relay characteristic along the line designated as U. V_T phasor controls the relay characteristic along the line designated as "T". "V_U" phasor consists of reversed relay terminal voltage (V) phase shifted by 90° and modified by compensator output -jI R . R represents the reach of the compensator designated as "$-T_{AB}$" that is set for the desired value "R_U" along the R-axis. "V_T" vector consists of relay terminal voltage ("V") phase shifted by 90° and modified by compensator output $-jI_pR_T$

R represents the reach of the compensator designated as "+T_{AB}" that is set for the desired value "R_T", along the R-axis.

For a fault at point "P" (Fig. 7 (B) within the relay trip characteristic) the "-T_{AB}" compensator voltage I_pR_U is added to -jV phasor so that the sum of these two phasors results in a phasor V_U that lags the V_{OP} phasor fulfilling the tripping conditions. Since phasor V_T was already in the lagging condition and the compensator voltage from +T_{AB} compensator I_pR_T has only increased its magnitude without changing its relative position with respect to V_{OP}.

Fig. 7 (C) shows relay response to a fault at point "Q" (located beyond the relay characteristic) since there is not enough current to produce reversal of the V_U phasor there will be no tripping output because V_U phasor leads phasor V_{OP}.

Fig. 7 (D) shows similar relay response (no trip) for point "M" (located beyond the relay characteristic) since there is not enough compensation to cause phasor V_T to lag phasor V_{OP}.

Fig. 7 (E) shows the relay response to a fault at point "N". In this case relay response is similar to the point "P" response. The compensator output voltage I_nR_T is large enough to produce a phasor V_T that lags phasor "V_{OP}".

Fig. 7 (F) point "S" illustrates response of a 90° lag fault. When there is no fault current, the relay is inoperative since $V_{OP} = O$. In the presence of a small amount of current, V_{OP} appears and a small compensation makes V_T and V_U lag V_{OP} and produce a tripping condition.

Phase Angle Comparison Unit

Referring to Fig. 4 the phase angle comparison unit is tripped when current flows into the base of transistor Q27 through zener diode Z3. Such tripping current must come from the 20V bus through either transistor Q2 or Q4 located in the "operate" circuit. The operate circuit, driven by transformer T1, is continually trying to trip the unit by supply current through Q2 on alternate half cycles. Q2 on alternate half cycles. Q2 conducts when the polarity marked terminals of T1 are positive.

When Q2 conducts, a portion of the current goes through resistor R20. This current, I_{R20}, may take either of two paths to the negative bus. If QS1 is in a conducting state, I_{R20} passes through it directly to the negative bus. If QS1 is in a blocking state, I_{R20} passes through D43 and then through Z3 to transistor Q27 to cause tripping. Thyristor QS1 is located in the "polarizing circuit +1" of the relay. This circuit is driven by transformer T2.

To prevent the operate circuit from causing tripping, the polarity marked terminals of T2 must go positive before the polarity terminals of T1 do. This causes Q5 to conduct current through R16 and drive the base of Q9. Q9 then conducts current from the 13V bus through R19 to gate QS1 into conduction. When QS1 conducts, it short circuits the current which might otherwise pass through D43 to cause tripping. Once QS1 begins to conduct, the gate loses control and it remains in the conducting state until the current is turned off by Q2. No tripping output can develop as long as the T2 voltage leads the T1 voltage.

The operate circuit switches for the next half cycle so that transistors Q3 and Q4 conduct in an attempt to cause tripping. In the polarizing circuit, Q6, Q10, and QS2 seek to prevent tripping by short circuiting the current which might otherwise pass through D44, Z3, and Q27.

Polarizing unit marked "-1" provides similar action as unit "+1".

Notice that QS3 and QS4 units provide similar action as QS1 and QS2. Since QS1 and QS3, and QS2 and QS4 units are connected in parallel, so that two tripping outputs per half cycle are needed to make operation of Q27 possible.

Polarizing boards marked "+2" and "-2" act in similar manner as the boards "+1" and "-1", except they control Q31 transistor that provides output for unit #2 (the outside characteristic lines).

Restraint Squelch

When the operate circuit transistor Q2 conducts, approximately 18V is applied through diode D25 to back bias D26 and prevents Q9 from turning on. Thus a trip signal, initiated because the T1 voltage is leading, cannot be improperly interrupted when the T2 voltage goes positive. A full half cycle tripping output is therefore produced by Q . This back biasing connection is called the restraint squelch

circuit. The same is true for D30, D29, and Q4 & Q10 on the alternate half cycle.

Similar function is performed by D55, D56, Q19 and D59, D60, Q20 board "+2" and D67, D68, and Q23, and D72, D71, Q24 on board "-2".

The operate circuit and the polarizing circuit are both duals having identical circuits which operate on alternate half cycles. The restraint squelch works into each of the duals in the same way.

Transformer T3 receives a polarizing signal from the circuit which is identical to the one that supplies transformer T2. The phase angle relation between the T1 voltage and the T3 voltage is compared in the same manner as described above and tripping signals are supplied through D44 and D43, through DZ3 and to Q27. This polarizing circuit contains a restraint squelch identical to one described for the T2 circuit.

D.C. Voltage Detector

Transistor Q25 and zener diode Z7 for output #1, and Q29 and zener diode Z9 for output #2 monitor D.C. voltage level. If the d-c voltage drops too low for the logic to operate properly, it will cause Q25 or Q29 in turn off and thereby send a gate signal to the restraint thyristors through D27, D28 for output #1 and D58 and D57 for output #2.

Output Circuit

Output for unit #1 is provided by Q26 (Relay terminal #5) and for unit #2 by Q30 (Relay terminal #6.) The output transistor provide 15 to 19 V. d.c. and up 0.010 amperes d.c.

The operation of Q26 and Q30 transistor is effected when tripping signals provided by relay logic operate transistor Q27 for output #1, and Q31 for output #2.

CHARACTERISTICS

* The relay is energized by phase-to-phase voltage and wye current. The compensators are connected to give the effect of the difference of the 2 phase currents.

Tap plate settings are related to the characteristics of the relay as shown in Fig. 6 as follows:

T2 and U2 represent characteristic of unit #2, and T1 and U1, represent characteristic of unit #1.

+TA1, +TA2, +TB1, and +TB2 values represent compensator tap settings.

Relay tap setting "T" relates to "R" component on the R-X diagram for different maximum sensitivity angle compensation as follows:

for	90°	- angle	R = 1.0T
	75°	- angle	R = 1.04T
	60°	- angle	R = 1.12T

* The relay is shipped with maximum sensitivity angle of 75° and can be readjusted continuously between 60° and 90°, as outlined in calibration procedure.

All tap plate settings can be set independently.

Tap plate markings are as follows:

1.51 2.00 2.50 3.50 5.00 7.10 10.00

Sensitivity

A plot of relay reach in per cent of tap block setting vs. relay terminal voltage at 0 degrees is shown on Fig. 8.

Time of Operation

The operating time of the relay varies from 2 msec. to 9 mseconds for faults near the balance point.

CURRENT CIRCUIT RATING IN AMPERES

TAP SETTING	CONTINUOUS	1 SECOND
10.0	5.	240
7.1	6	240
5.0	8	240
1.51-3.50	10	240

Burden Data

Current Burden (Per Phase)
Measured at 5 amp/ 0 and Voltage 120 /0 applied to relay.

TAP SETTING	IMPEDANCE	RESISTANCE	REACTANCE
T	Z	R	X
10.0	.364 ohms	.252 ohms	.262 ohms
7.1	.224	.172	.144
5.0	.158	.133	.086
3.5	.116	.103	.053
2.5	.094	.086	.038
2.0	.084	.077	.033
* 1.51	.076	.071	.028

Potential Circuit Burden

At 120/ 0° volts and current circuits energized with 5/0° amps. the potential burden is 30 volt-amperes, 16.8 watts and 24.9 vars.

D.C. Current Burden

D.C. current burden is 0.07 amperes at all rated d.c. voltages.

SETTING THE RELAY AND CALCULATIONS

Relay reach is set on the tap plate. The tap plate markings are:

$$+T_{A1} + T_{B1} + T_{A2} + T_{B2}$$

$$-T_{A1} - T_{B1} - T_{A2} - T_{B2}$$

1.51 2.00 2.50 3.50 5.0 7.1 10.0

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angle 65° or higher. For line angles below 65° recalibrate for 60° - maximum sensitivity angle.

The tap plate settings (T) represent the reach perpendicular to maximum sensitivity angle and can be converted to the reach along the R-axis as follows:

for 90° - calibration R = 1.0T

75° - calibration R = 1.04T

60° - calibration R = 1.12T

Settings of $+T_{A1}$, $T_{B1} - T_{A1}$ and $-T_{B1}$ control the inside (#1) characteristic of the relay.

$+T_{A1}$ and $+T_{B1}$ control the reach along "+R" axis.

$-T_{A1}$ and $-T_{B1}$ control the reach along "-R" axis.

$+T_{A2}$, $+T_{B2}$, $-T_{A2}$, and $-T_{B2}$ controls the outside (#2) characteristics of relay.

"$+T_{A2}$ and $+T_{B2}$ control the reach along "+R axis.

$-T_{A2}$ and $-T_{B2}$ control the reach along "-R" axis.

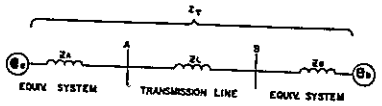
Letter "A" refers to phase "A" setting and letter "B" to phase B setting. All "+T" settings can be made independently from "-T" settings if required.

Compensator Setting

Each set of compensator taps terminates in in inserts which are grouped on a socket and form approximately three quarters a circle around a center insert which is the common connection for all of the taps. Electrical connections between common insert and tap inserts are made with a link that is held in place with two connector screws, one in the common and one in the tap. There are two T_B settings to be made since phase B current is passed through two compensators. A compensator tap setting is made by loosening the connector screw in the center. Remove the connector screw in the tap end of the link, swing the link around until it is in position over the insert for the desired tap setting, replace the connector screw to bind the link to this insert, and retighten the connector screw in the center. Since the link and connector screws carry operating current, be sure that the screws are turned to bind snugly.

Setting Example

CRITERION FOR SETTING BLINDERS FOR OUT-OF-STEP RELAYING



Z_A, Z_L, Z_B = Primary ohms

1. Inner blinder must be set to accommodate maximum fault resistance for internal 3-phase fault.

2. Inner blinder should not operate on most severe stable swing.

3. Outer blinder must have adequate separation from inner blinder for fastest out-of-step swing to be acknowledged as an out-of-step condition.
4. Outer blinder must not operate on load.

Inner Blinder Setting

A reasonable approximation of arc resistance at fault inception is 400 volts per ft. If a maximum ratio (line voltage/ (spacing) is 10,000 volts per ft. for a high voltage transmission line and if a min. internal 3-phase fault current is calculated as:

$$I_{min} = \frac{E}{(Z_A + Z_L)\sqrt{3}}$$ where Z_A is maximum source impedance Z_L is line impedance, and E is line-to-line voltage.

Then: $R_{max} = \frac{400 \times Ft.}{I_{min}} = \frac{400 \times Ft}{E}\sqrt{3}\ (Z_A + Z_L)$

$$R_{max} = \frac{693}{10{,}000}(Z_A + Z_L) = .0693\,(Z_A + Z_L) \quad (1)$$

Adding a 50% margin to cover the inaccuracies of this expression.

$$R_{max} = 0.104\,(Z_A + Z_L)$$

$$\text{Secondary ohms} = R_{max}\frac{R_C}{R_V} = R_S$$

where R_C - C.T. Ratio

R_V - P.T. Ratio

If the relay has maximum sensitivity angle setting of 75°, then relay tap setting $T = \frac{R_S}{1.04}$

Use next higher T-compensator setting ($+T_{A1}$, $+T_{B1}$ and $-T_{A1} - T_{B1}$). This setting controls #1 unit reach.

This is the minimum permissible inner blinder setting where it is used to provide a restricted trip area for distance relay.

* Another criterion that may be considered is based upon the rule of thumb that stable swings will not involve an angular separation between generator voltages in excess of 120 degrees. This would give an approximate maximum of:

$$Z_{inner} = \frac{Z_A + Z_L + Z_B}{2\ \sqrt{3}} = .288\,(Z_A + Z_L + Z_B) \quad (2)$$

where Z_B is the equivalent maximum source impedance at the end of the line away from Z_A.

In terms of secondary ohms

$$Z_{inner\ (secondary)} = \frac{R_C}{R_V} Z_{inner} \quad (3)$$

In this case Z (secondary) - directly corresponds to the T - tap plate setting without conversion from R-setting. Use the nearest T-setting.

In this case again T-setting to be used are for #1 unit ($+T_{A1} + T_{B1} - T_{B1} - T_{B1}$).

An inner blinder setting between the extremes of (1) and (2) may be used. This provides operation for any 3-phase fault with arc resistance, and restraint for any stable swing. Except in those cases where very fast out of step swings are expected the larger setting can be used.

For slow out-of-step swings a reasonably close placement of this outer to the inner blinder characteristic is possible. The separation must however be based on the **fastest** out-of-step swing expected. A 50 millisecond interval is inherent in the out-of-step sensing logic and the outer blinder must operate 50 ms or more ahead of the inner blinder.

Since the rate of change of the ohmic value manifested to the blinder elements is dependent upon accelerating power and system WR^2 it is impossible to generalize. However, based on an inertia constant (H) equal to 3 and the severe assumption of full load rejection, a machine will experience, assuming a uniform acceleration, an angular change in position of no more than 20 degrees per cycle on the first half slip cycle.

Outer Blinder Setting

If the inner blinder were set for 0.104 ($Z_A + Z_L + Z_B$) and the very severe 20 degrees per cycle were used, the simple trigonemetric manipulation of Appendix I reveals that the outer blinder should be set for approximately:

$$Z_{outer} = 0.5\,(Z_A + Z_L + Z_B)\ (\text{Primary}) \quad (4)$$

Note that the 0.104 ($Z_A + Z_L + Z_B$) expression includes Z_B which was not present in the minimum relationship. **Using** the actual minimum for the inner blinder setting provides further margin.

It will usually be possible to use the minimum blinder setting of 1.5 ohms (secondary). Based on the 20 ohm per cycle criterion and the logic requirement of 50 milliseconds, Appendix II and Appendix III show the method of calculating the outer blinder setting.

It should be recognized that with the OS-2 logic, no commitment to trip on out-of-step occurs until the inner blinder operates. Therefore, a stable swing for which the outer blinder operates imposes no problem.

Also it should be emphasized that if a distance relay were used to supervise the out-of-step relaying, the distance relay 3-phase element and the inner blinder would have to operate for 20 milliseconds in order for tripping to take place on an out of step condition. This may require a somewhat longer reach on the distance relay than would otherwise be required. For the calculation of Appendix II or Appendix III the result is in terms of secondary ohms and corresponds to T-tap plate setting without conversion. Use the next highest T-setting.

Set $+T_{A2}$, $+T_{B2}$, $-T_{A2}$, $-T_{B2}$ (unit #2 settings) for outside blinder settings.

Line Angle Adjustment

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65° set for a 60° maximum sensitivity angle by adjusting the pteentiometer P1. Refer to calibration procedure when a change in maximum sensitivity angle is desired.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay by menas of the four slotted holes on the front of the case. Additional support should be provided toward the rear of the relay in addition to the front panel mounting. This will protect against warping of the front panel due to the extended weight within the relay case.

EXTERNAL CONNECTIONS

Figure 9 shows the external connections for an SDBU-2 relay.

Current circuit connections are made to an eight section terminal block located at the rear. Potential circuits, both a-c and d-c as well as input and output logic signal circuits, are connected through a 24-terminal jack. Connections are made by a plug on the wiring harness. The plug is inserted between the two latching fingers which hook over the back of the plug to prevent an accidental loosening of the plug. The plug can be removed by spreading the two fingers apart enough to disengage the hooks from the back. The plug must be withdrawn while the fingers are spread apart.

Note that terminal number 1 is connected to the case within the relay and may be used for grounding the shields of connecting cables. The grounding connection will be broken when the plug is disconnected.

Permanent grounding of the case is accomplished by connecting a ground wire under a washer of a cover screw. These are self-tapping screws and provide excellent low resistance contact with the case.

RECEIVING ACCEPTANCE

1. Give visual check to the relay to make sure there are no loose connections, broken resistors, or broken wires.
2. Perform electrical acceptance test that consists of an electrical test to make certain that the relay measures the balance point impedance accurately, and hi-pot tests.

Recommended Instruments for Testing

Westinghouse Type PG-161 - S#291B749A33 or equivalent a.c. voltmeter.

Westinghouse Type PA-161 - S#291B719A21 or equivalent a.c. ammeter.

Hi-Pot Tests

CAUTION: Before making Hi-Pot tests, connect together jack terminals 3, 4, 5, 6 to avoid destroying components in the static network. These connections are not necessary for surge testing. Besides, connect together jack terminals 7 & 8.

Electrical Tests

The test for distance unit is accomplished by use of test connections shown in Fig. 16. Tripping is indicated by a voltmeter reading connected to the output terminals. At the balance point, the voltmeter reading may be as low as 1 volt or 2 volts d.c. indicating that the system is only tripping during a part of a cycle. This is normal balance point characteristic; however, an increase in current over 5 per cent should produce output of 15 to 21 volts d.c. A reading less than 12 volts indicates a defective tripping output. When checking current and voltage limits allow for additional instrumentation errors.

Set relay for all T = 10.0

Step 1. Monitor output #1 at Varicon terminals "5" and output #2 at Varicon terminals "6". Apply 40 volts ac to Varicon terminals "7" and "8" with polarity mark on terminal "7" apply a-c current into current terminal "5" out current terminal "7" (jumper terminals "8" and "6" together).

Apply rated d-c voltage to Varicon terminals "4" and "3" with positive on "4".

a) Set phase shifter at 40° current lagging voltage. The trip current should be between 1.11-1.19 amps.

b) Set phase shifter for 290° current lagging voltage. The trip current should be 1.12-1.18 amps.

Step 2. Reverse current connections to terminals "5" and "7". Repeat step 1, monitoring output #1 and #2.

Step 3. Set phase shifter for 345° current lagging voltage. Monitor outputs #1 and #2. Relay should operate between 1.92 and 2.12 amperes.

Step 4. Move current lead from terminal "7" to terminal "6". Tripping current on both units should be between 3.84-4.24 amp.

Step 5. Reconnect current circuit with current into terminal "5" out terminal "7" ("6" and "8" jumpered). Set voltage for 125 volts a.c., current 75° lagging. Check outputs #1 and #2 operating current should be below 0.400 amp. at some point between 73° and 78°.

Step 6. Reverse current connections to terminals "5" and "7" and repeat Step 5.

If some other T-setting than T=10 is used for testing the current values should be obtained by using following equation.

$$I_{test} = \frac{V}{2T} \cos (90 - \beta + d) \ (\pm 4\%)$$ where $\propto$ is angle by which current lags the voltage and β is the desired minimum torque angle. For factory calibrated relays, $\beta = 75°$ current is taken as reference at 0°.

If the electrical response is radically outside the limits after making allowance for instrumentation error (particularly the phase angle meter error is of critical importance). Relay should be recalibrated as outlined in the section under "Calibration Procedure."

ROUTINE MAINTENANCE

The relays should be inspected periodically, at such time intervals as may be dictated by experience, to insure that the relays have retained their calibration and are in proper operating condition.

REPAIR CALIBRATION

Use the following procedure for calibrating the the relay if the relay has been taken apart for repairs or the adjustments disturbed. For best results in checking calibration the relay should be allowed to warm up for approximately one hour at rated voltage. However, a cold relay will check to within two per cent of the warm relay.

Settings

A. Set all compensators on T = 10.

B. Make following potentiometer settings:

NOTE: Loosen locknuts before rotating the brush. The locknuts should be retightened when calibration is completed.

P2 - Connect ohmmeter to the middle (brush) terminal and the free termi-

nal (without any connections), and adjust potentiometer for approximately 2000 ohms.

P1, P3, P4, P5 - Should be set in maximum clockwise position.

Electrical Tests and Connections

A. Calibrate phase shifter using wattmeter method of 90° current lagging voltage for 0-watts reading, and at 60°. The watts at 60° should read one-half of the maximum watts reading obtained on the wattmeter at 0° setting.

B. Output from unit #1 is observed between varicon terminals #5 and #3, and for output from unit #2 between Varicon terminals #6 and #3. Monitor relay output using high impedance (at least 20,000 ohms/volt) d-c voltmeter suitable for reading 0-25 volts d-c. Consider as positive relay output voltmeter deflection of 5 volts or more. Then, increase current slightly beyond the limits for full 18-20 volts d-c output.

C. Apply a-c voltage to Varicon terminals "7" and "8" with polarity mark on terminal "7."

D. Apply a-c current into current terminal "5" out current terminal "7" (jumper terminals "8" and "6" together).

E. Apply rated d-c voltage to Varicon terminals "4" and "3," with positive on "4 ".

RELAY CALIBRATION

Calibration angles are given for maximum torque angle $\beta = 75°$. For $\beta \neq 75°$ modify test angles by $[-(75° - \beta)]$.

A. Apply 40 volts a-c and 1.15 amp. of a-c current. Set phase shifter at 40° current lagging voltage. Adjust P1 until output #1 is first obtained, and then just resets.

B. Set phase shifter for 290° current lagging voltage. Set current for 1.15 amp. and voltage for 40 volts a-c. Adjust P2 until an indication of output #1 is obtained.

C. Repeat step A.

D. Recheck step B: If P2 adjustment was needed, then recheck step A; if no P2 adjustment was needed, lock P1 and P2. If P1 adjustment was needed repeat step B. In general, repeat steps A and B again until P1 and P2 readjustments are not needed. Lock P1 and P2.

E. Monitor output #2. Adjust P4 until trip current is 1.12-1.15 for 40 volts a-c at 40° and 290° current lagging.

F. Reserve current connection to terminals "5" and "7" and repeat step E. Adjust P5 to meet limits.

G. Monitor output #1. Adjust P3 until trip current is 1.15 amp. at 40° current lagging and 1.15 amp. at 290° (±1°) current lagging.

H. Set phase shifter for 345° current lagging 40 volts a-c. Check outputs #1 and #2. Current limits should be 1.94-2.10 amps. Apply current into terminal "5" out "6" only. Check outputs #1 and #2. Current limits should be 3.88-4.20 amperes.

Apply current to terminals "8" and "7" only with polarity on "8". Check outputs #1 and #2. Current limits should be 3.88-4.20 amperes.

I. Connect current again into term. "5" out terminal "7" (terminals "8" and "6" should be jumpered together). Set phase shifter for 75° current lagging 120 volts A-C. Check outputs #1 and #2. Operating current should be below .400 amps. between 73° and 78°.

J. Set phase shifter for 165° current lagging, and repeat step "H".

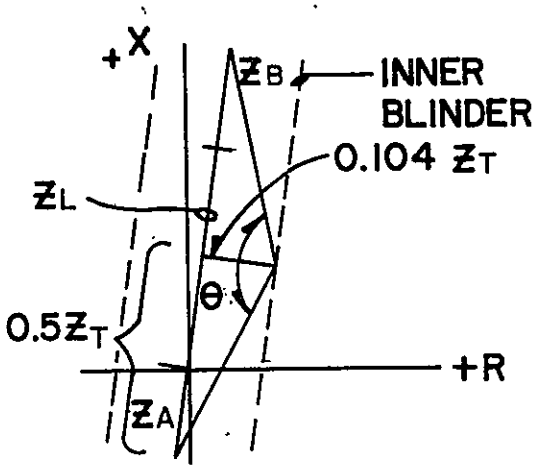
K. Connect current into term. "5" out term. "7" (terminals 6 and 7 jumpered together).

L. Set phase shifter for 255° current lagging 120 volts a-c- Check outputs #1 and #2. Operating current should be below .400 amps between 255° and 257°.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give the circuit symbol, electrical value and style number.

APPENDIX I – Determination of Outer Blinder Setting with Inner Blinder Set for 0.104 ($Z_A + Z_L + Z_B$) in terms of primary ohms.

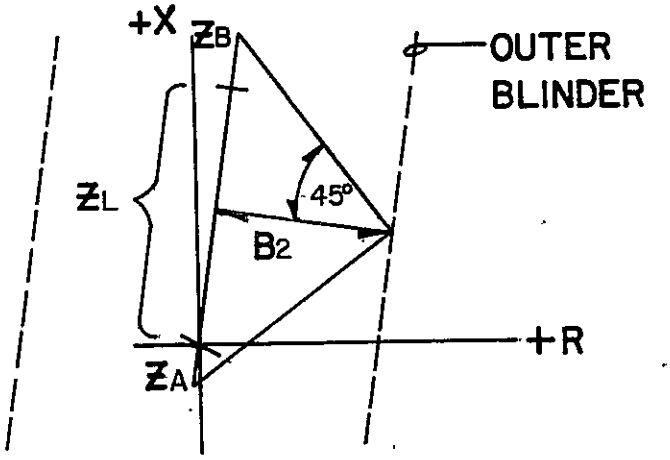


$$\theta = 2\tan^{-1}\frac{0.5}{0.104} = 2\tan^{-1}(4.8)$$

$$\theta = 2\,(78.2) = 156.4^\circ$$

With a 20° per cycle swing rate and a 50 milliseconds logic criterion, the limiting swing angle between blinder operations is 20 x 3 = 60 degrees.

$$\frac{\theta - 60}{2} = \frac{156.4 - 60}{2} = 48.2^\circ$$



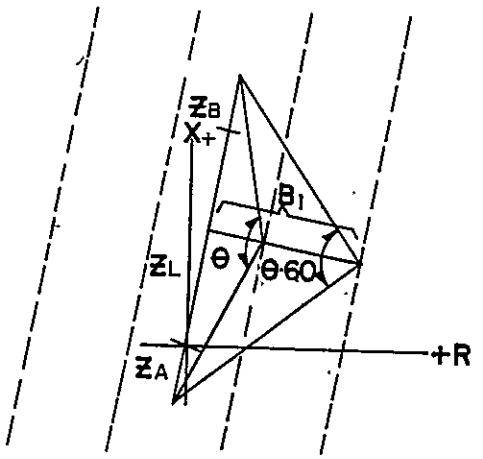
$$B_1 = \frac{Z_A + Z_L + Z_B}{2\tan 48.2^\circ} = 0.448(Z_A + Z_L + Z_B)$$

Use $Z_{outer} = 0.5\,(Z_A + Z_L + Z_B)$ Primary ohms.

This is the minimum setting of the outer blinder for 20 degree per cycle swing rate.

APPENDIX II – Determination of Outer Blinder Setting with Inner Blinder Set for 1.5 Ohms (secondary) and $\frac{Z_T R_C}{3 R_V} \geq 0.8$ where $Z_T = Z_A + Z_L + Z_B$ (primary ohms) R_C is Current Transformer Ratio and R_V is Potential Transformer Ratio.

At 20 degrees per cycle swing rate and 50 millisecond logic criterion the limiting swing angle between blinder operations is 20 x 3 = 60 degrees.



$$\tan\left(\frac{\theta - 60}{2}\right) = \frac{Z_T}{2B_1}$$

$$B_1 = \frac{Z_T}{2}\left[\frac{1}{\tan(\theta/2 - 30)}\right]$$

$$B_1 = \frac{Z_T}{2}\left[\frac{1 + \tan\theta/2 \tan 30}{\tan\theta/2 - \tan 30}\right]$$

$$B_1 = \frac{Z_T}{2}\left[\frac{1 + 0.577 \tan\theta/2}{\tan\theta/2 - 0.577}\right]$$

$$B_1 = \frac{Z_T}{2}\left[\frac{\sqrt{3} + \tan\theta/2}{\sqrt{3}\tan\theta/2 - 1}\right]$$

$$\text{but } \tan\theta/2 = \frac{Z_T R_C}{2(1.5) R_V} = \frac{Z_T R_C}{3 R_V}$$

Use Z_{outer} (Pri) = 1.1 B_1 to provide additional margin.

$$Z_{outer}\ (Sec.) = 1.1\ B_1 \frac{R_C}{R_V}$$

This is the minimum setting of the outer blinder for 20 degree per cycle swing rate.

APPENDIX III – Determination of Outer Blinder Setting with Inner Blinder set for 1.5 ohms (secondary) and $\frac{Z_T R_C}{3 R_V} < 0.8$ where $Z_T = Z_A + Z_L + Z_B$ (primary ohms), R_C is C.T. Ratio and R_V is P.T. Ratio.

Calculate $\theta = 2 \tan^{-1} \frac{Z_T R_C}{3 R_V}$

Using maximum swing rate, K (degrees per cycle), calculate:

$$B_1 = \frac{Z_T}{2}\left[\frac{1}{\tan 1/2\,(\theta - 3K)}\right]$$

Set Z_{outer} (primary) = 1.1 B_1

This is the minimum setting in primary ohms) of the outer blinder for the maximum swing rate K.

TABLE I

NOMENCLATURE FOR RELAY
Type SDBU-2

ITEM	DESCRIPTION		
CA1	1.1 Mfd. Capacitor	S# 14C9400H21	
CA2, CA3, CA4, CA5	0.6 Mfd. Capacitor	14C9400H10	
DZP	Zener Regulating Diode 1N2984B		
PRINTED CIRCUIT BOARDS			
Operating Board		S# 899C632G01	Fig. 10
Polarizing Board "+1"		899C633G01	Fig. 11
Polarizing Board "-1"		899C634G01	Fig. 12
Polarizing Board "+2"		899C635G01	Fig. 13
Polarizing Board "-2"		899C636G01	Fig. 14
Output Board		899C637G01	Fig. 15
RHEOSTATS			
P1	25 Watts, 5000 Ohms	S# 836A635H06	
P2, P3, P4, P5	25 Watts, 5000 Ohms	836A635H02	
RESISTORS			
R_{DC}	48V dc 40W 400 Ohms	S# 1955579	
	125V dc 40W 1500 Ohms	1955645	
R_{1A}, R_{2A}, R_{3A}, R_{4A}, R_{5A}	25 Watts, 2129 Ohms	1210089	
X_{A2}, X_{A3}, X_{A4}, X_{A5}	Phase Shifting Transformers		
I_{pol}, $+T_{A1}$, $+T_{B1}$, $-T_{A1}$, $-T_{B1}$, $+T_{A2}$, $+T_{B2}$, $-T_{A2}$, $-T_{B2}$	Compensators Assembly		
T_1, T_2, T_3, T_4, T_5	Coupling Transformers		

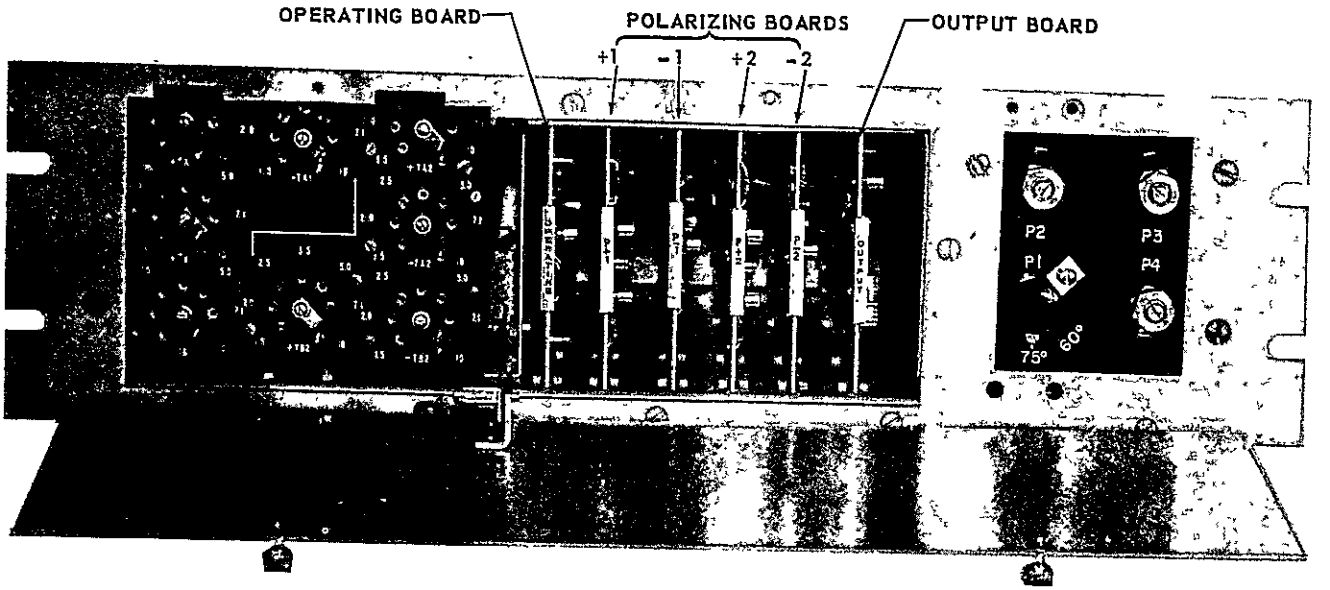


Fig. 1. Photograph of the Relay

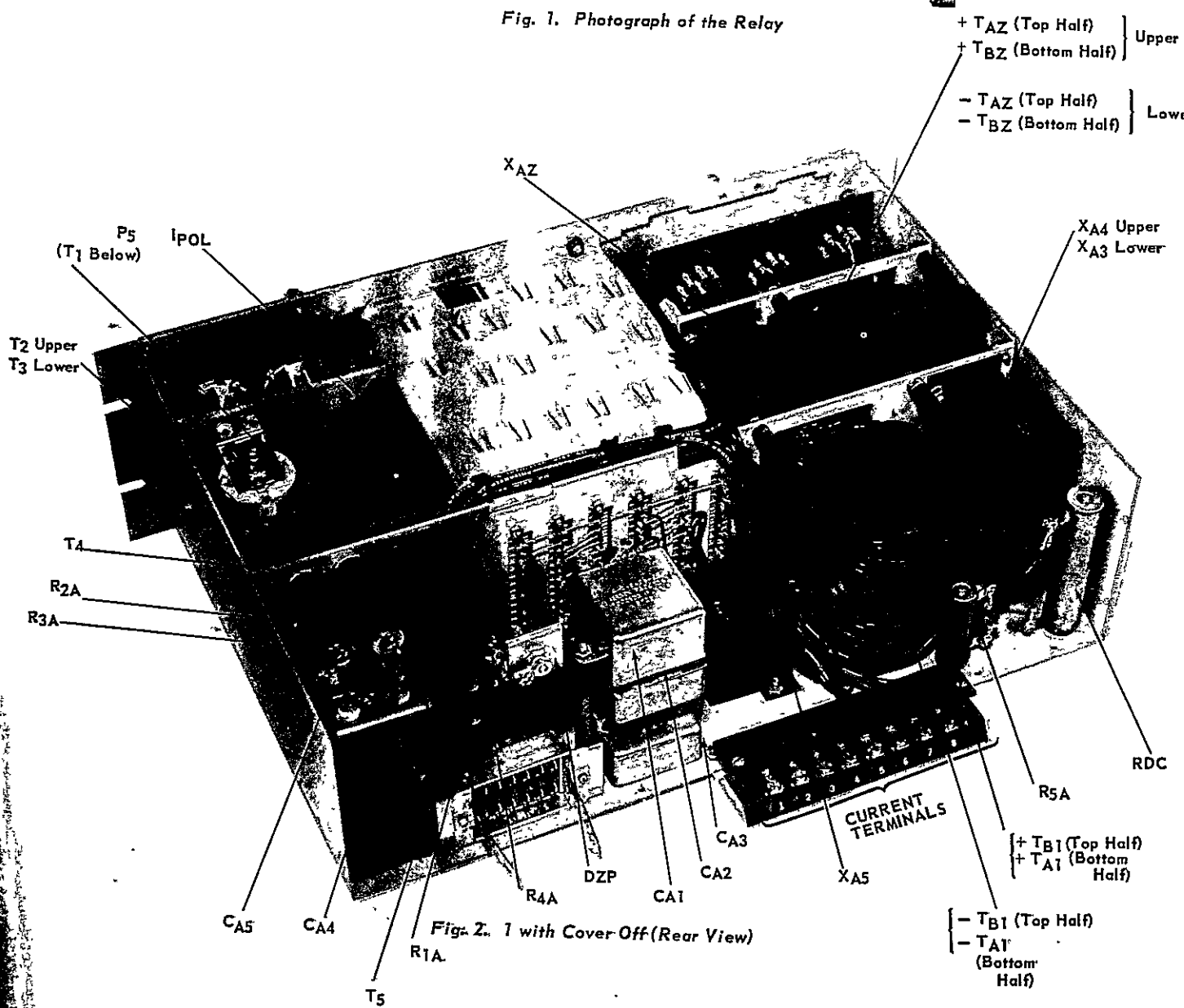


Fig. 2. 1 with Cover Off (Rear View)

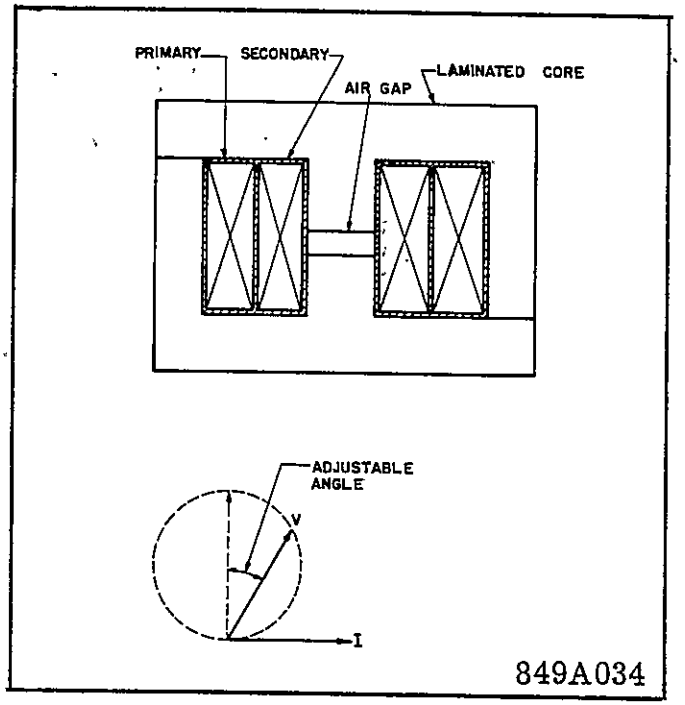


Fig. 4. Compensator Construction

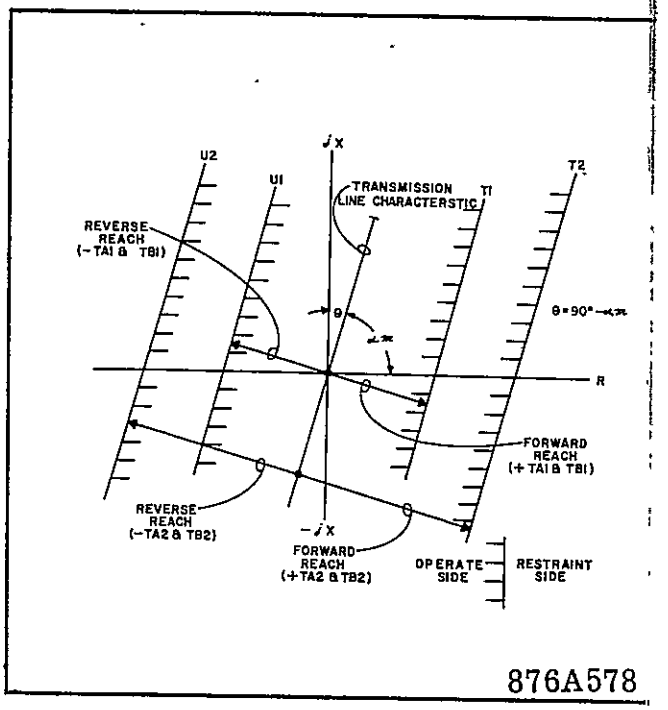


Fig. 5. SDBU-2 Relay R-X Diagram Characteristics

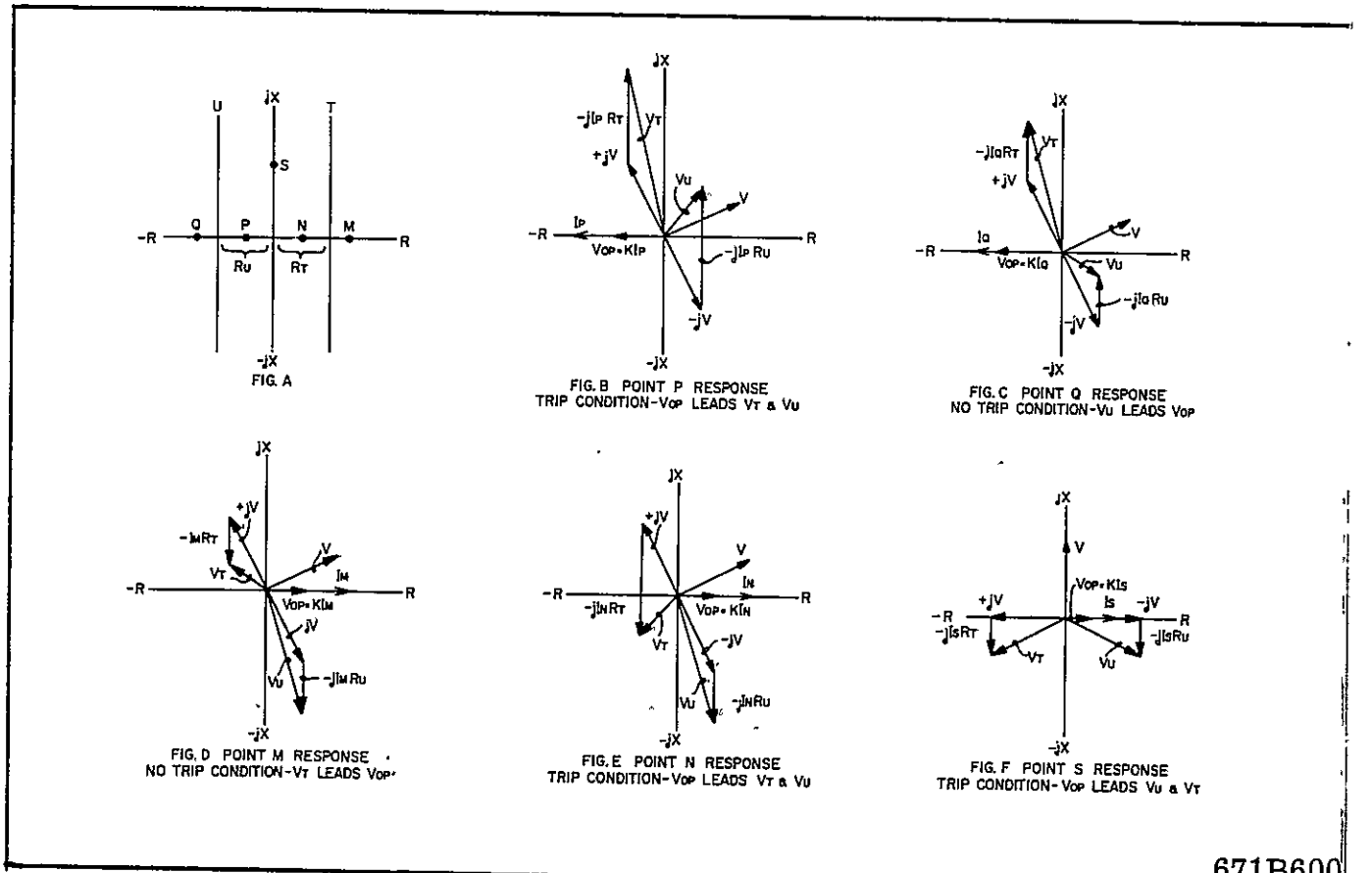
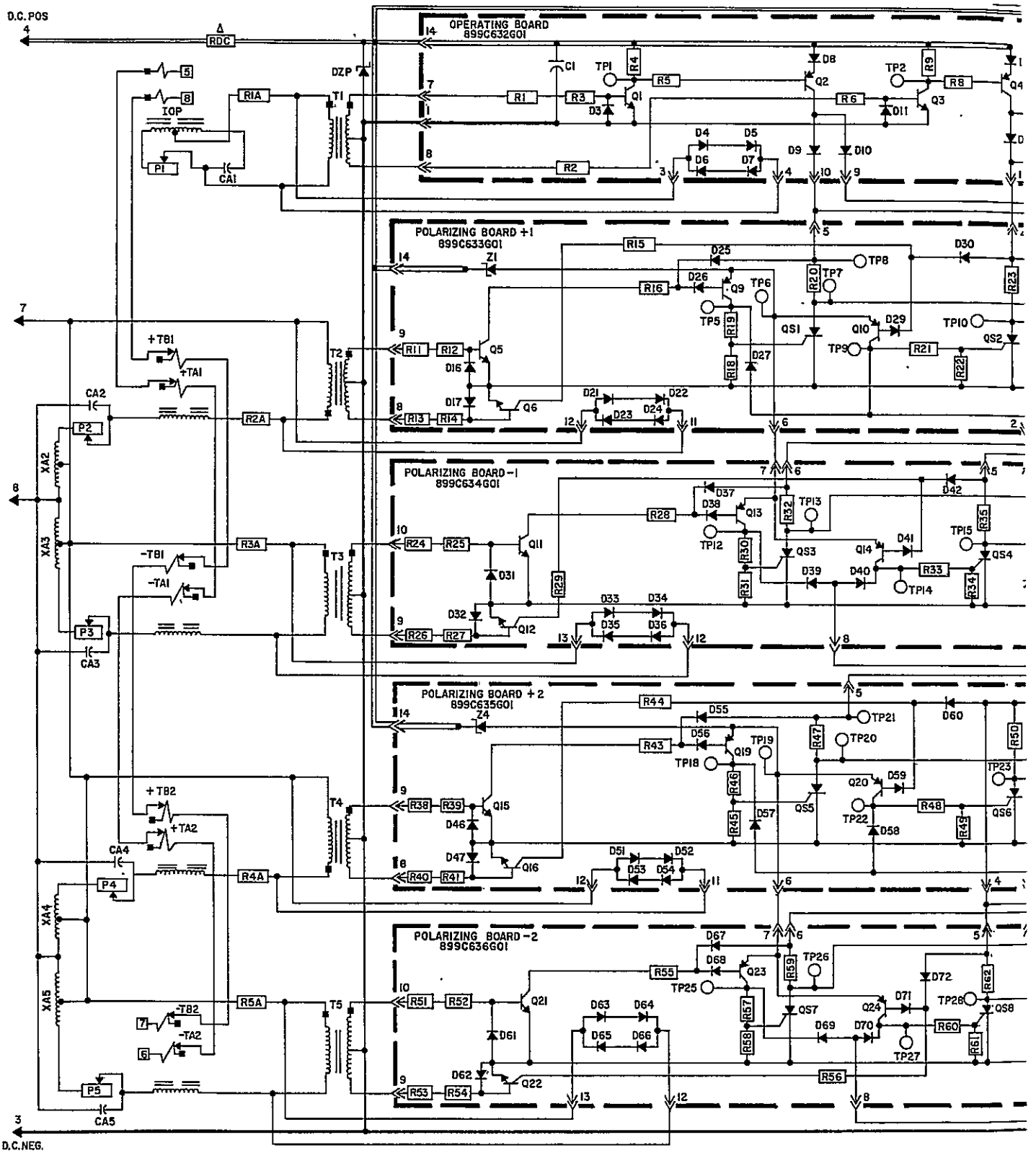
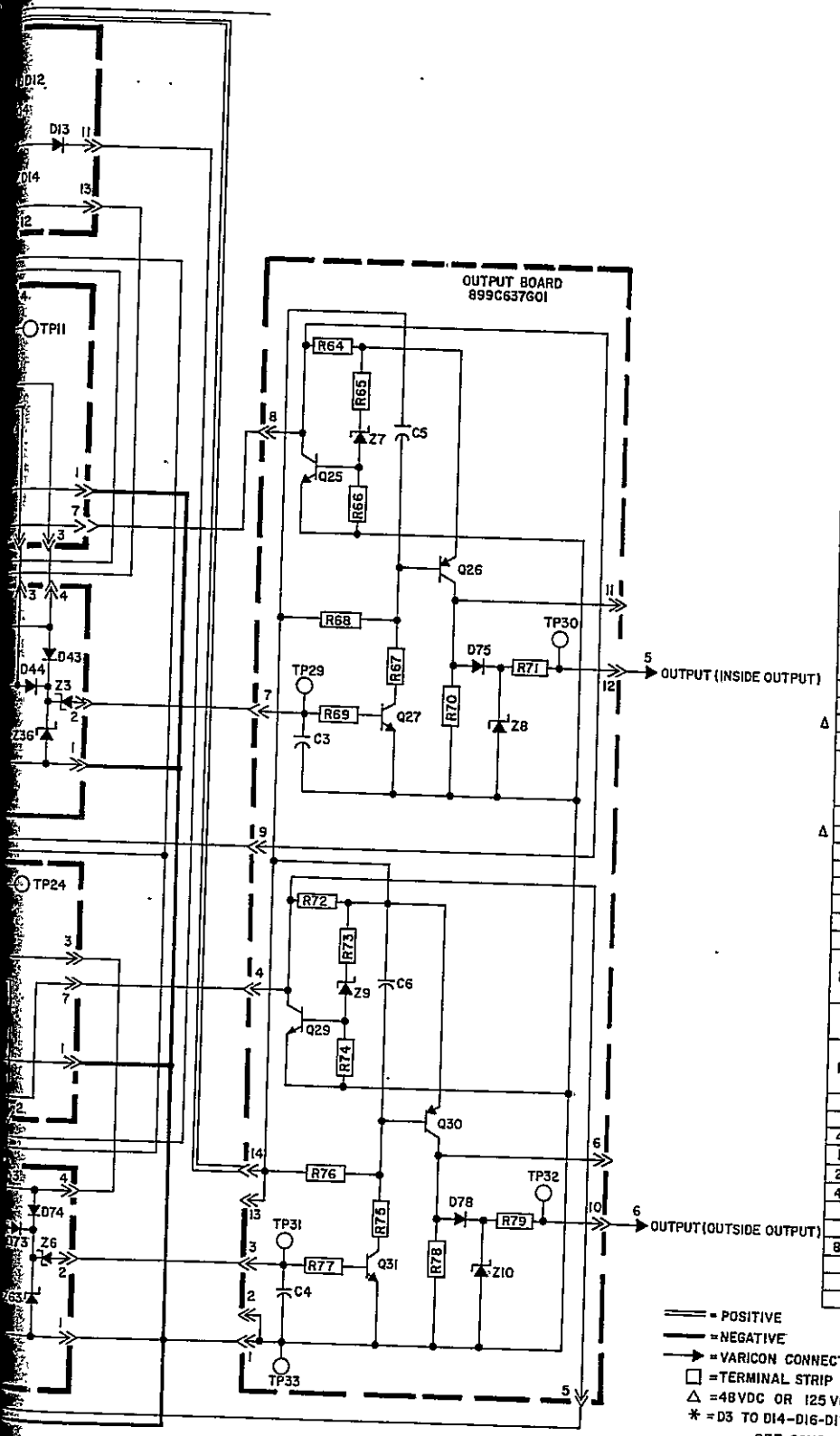


Fig. 6. SDBU-2 Phasor Relationship for Selected Conditions



* Fig. 3. Internal Schematic



REQ		CAPACITOR	STYLE NO.	REF.
1		C1	187A508H10	(18 MFD.)
2		C3-C4	187A624H10	(.015 MFD.)
1		CA1	14C9400H21	(1.1 MFD.)
4		CA2 TO CA5	14C9400H10	(.6 MFD.)
2		C5-C6	188A699H05	(.27 MFD.)
		DIODE		
64		*	188A342H06	(IN4818)
2		D75-D78	837A692H03	(IN645A)
		POTENTIOMETER		
4		P2 TO P5	836A635H02	(5000Ω 25W)
1		P1	836A635H06	(5000Ω 25W)
		RESISTOR		
2		R1-R2	184A763H77	(120K 1/2W)
2		R4-R9	184A763H99	(1 MEG 1/2W)
2		R66-R74	184A763H61	(27KΩ 1/2W)
1		R15	184A763H59	(22KΩ 1/2W)
2		R67-R75	629A531H52	(6.8K 1/2W)
2		R71-R79	762A679H01	(150Ω 3W)
2		R77-R69	184A763H69	(56KΩ 1/2W)
8		R19-R46-R21 R48-R30-R57 R33-R60	629A531H42	(2.7KΩ 1/2W)
2		R3-R6	184A763H75	(100KΩ 1/2W)
26		R18-R20-R22 R23-R24-R26 R31-R32-R34-R49 R35-R47-R50-R45 R51-R53-R58-R59 R62-R64-R72-R61 R11-R13-R38-R40	184A763H37	(2.7KΩ 1/2W)
9		R5-R8-R16 R56-R29-R28 R43-R44-R55	184A763H49	(8.2KΩ 1/2W)
2		R70-R78	629A531H78	(82K 1/2W)
5		R1A TO R5A	1210089	(2,120Ω 25W)
Δ 1		RDC (125 VDC)	1955645	(1,500Ω 40W)
2		R68-R76	629A531H56	(10K 1/2W)
8		R14-R39-R41 R25-R27-R52 R54-R12	184A763H03	(100Ω 1/2W)
2		R65-R73	184A763H57	(18KΩ 1/2W)
Δ 1		RDC (48VDC)	1955579	(400Ω 40W)
		TRANSFORMER		
1		T1	2928563G03	
4		T2 TO T5	2928563G02	
		TRANSISTOR		
10		Q1-Q3-Q5-Q6 Q11-Q12-Q15-Q16 Q21-Q22	848A851H01	(2N3391)
5		Q18-Q25-Q27 Q29-Q31	184A638H18	(2N697)
11		Q2-Q4-Q9-Q10 Q13-Q14-Q17-Q19 Q20-Q23-Q24	184A638H20	(2N1132)
		ZENER DIODE		
4		Z1-Z3-Z4-Z6	186A797H06	(IN957B)
1		ZP	762A631H01	(IN2984B)
2		Z8-Z10	862A288H01	(IN3688A)
4		Z7-Z9-Z36-Z63	186A797H01	(IN75B)
		SWITCH		
8		QS1 TO QS8	185A517H05	(2N884)

= POSITIVE
= NEGATIVE
= VARICON CONNECTOR
□ = TERMINAL STRIP
Δ = 48VDC OR 125 VDC
* = D3 TO D14-D16-D17-D21 TO D44-D46-D47-D51 TO D74
REF. COMP. LOC. – 671B641, 671B645,46,47,48 & 49.
MFG. REF. – 5303D96

5300D72

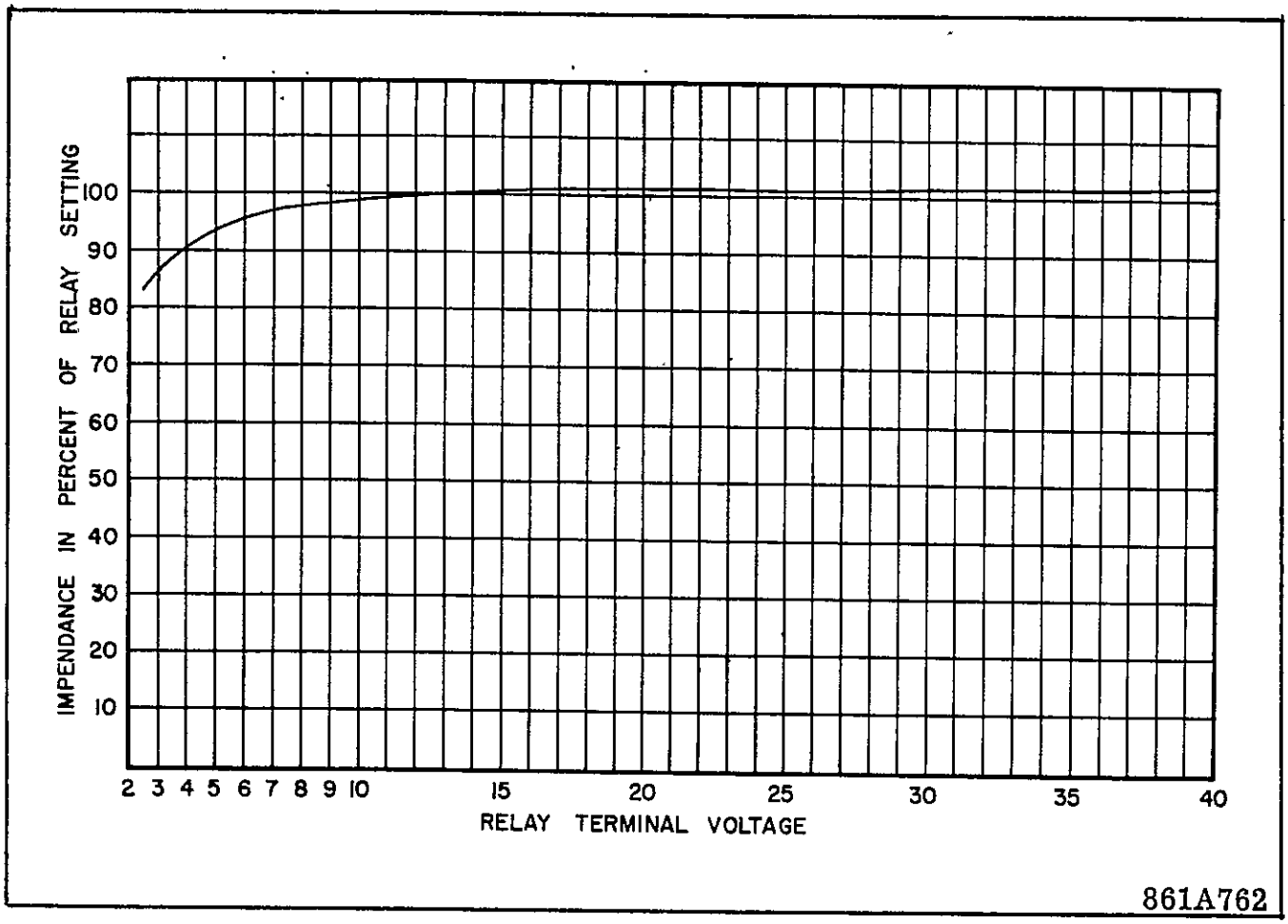


Fig. 7. Impedance Characteristics

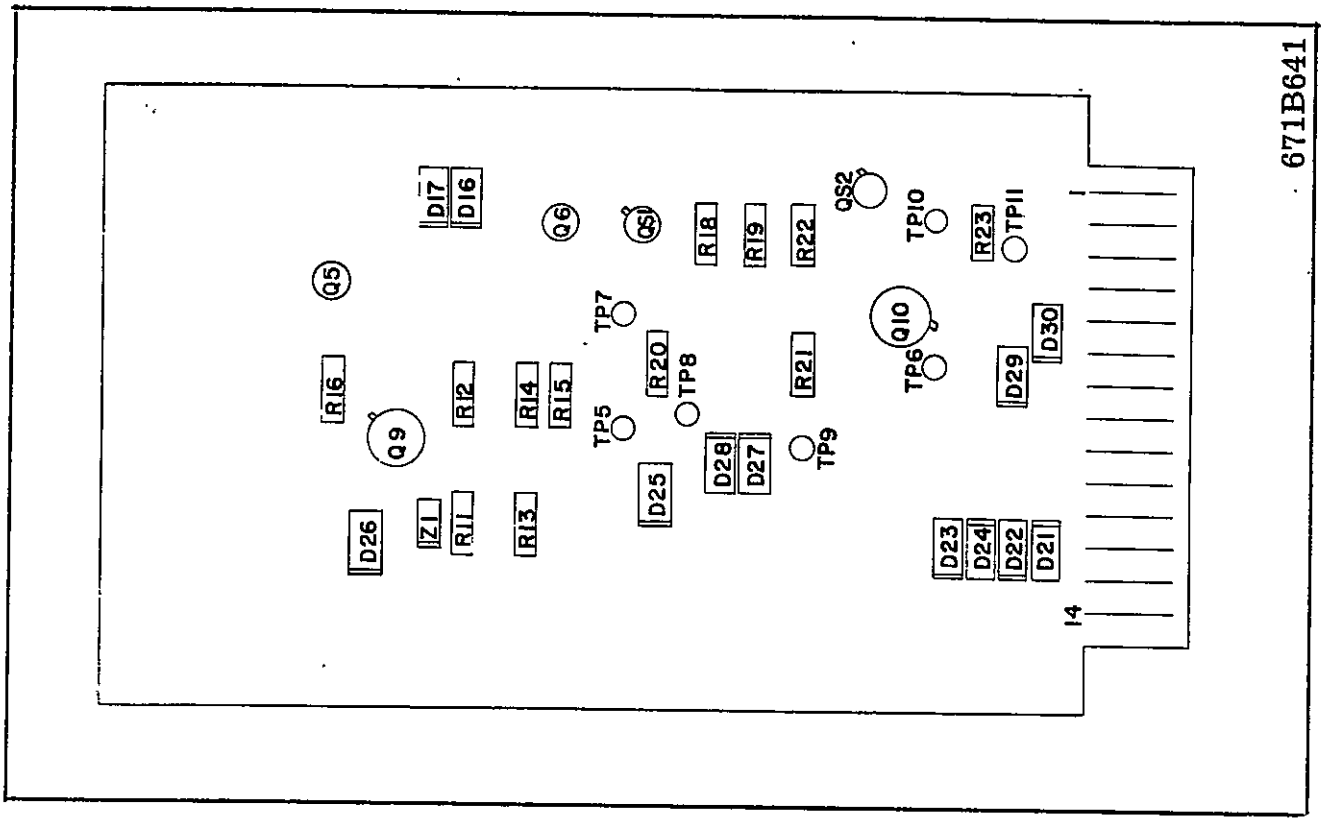


Fig. 10. Polarizing Board "+1"

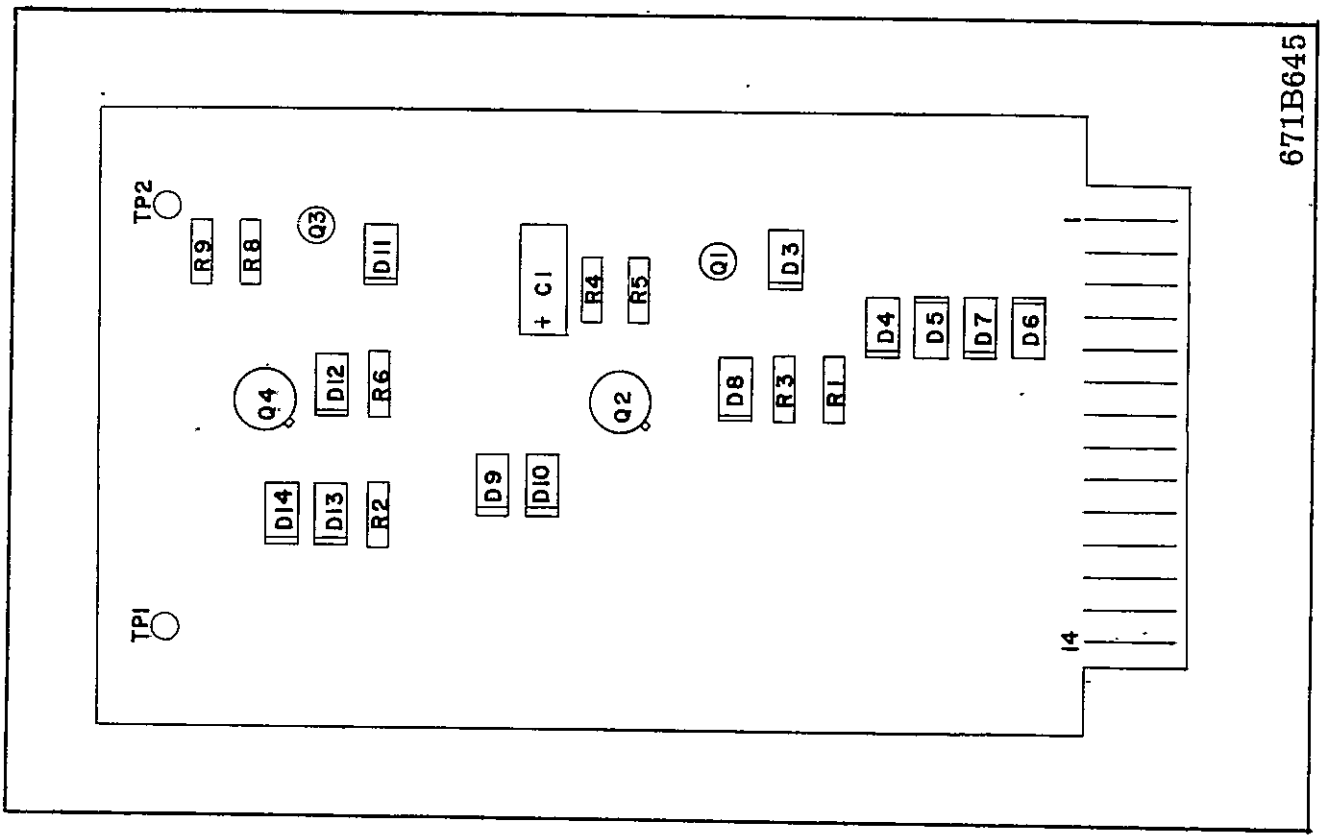


Fig. 9. Operating Board Printed Circuit

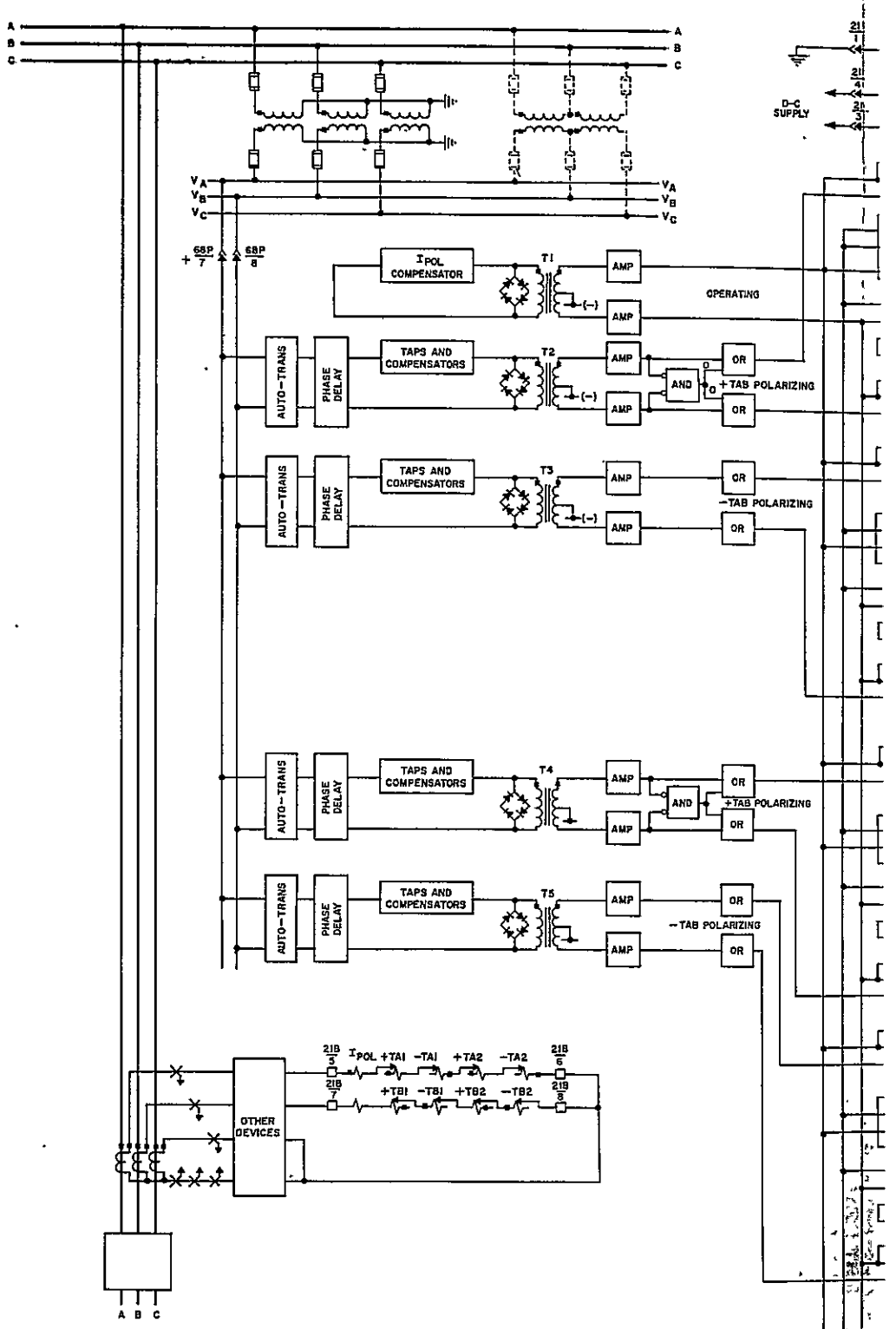
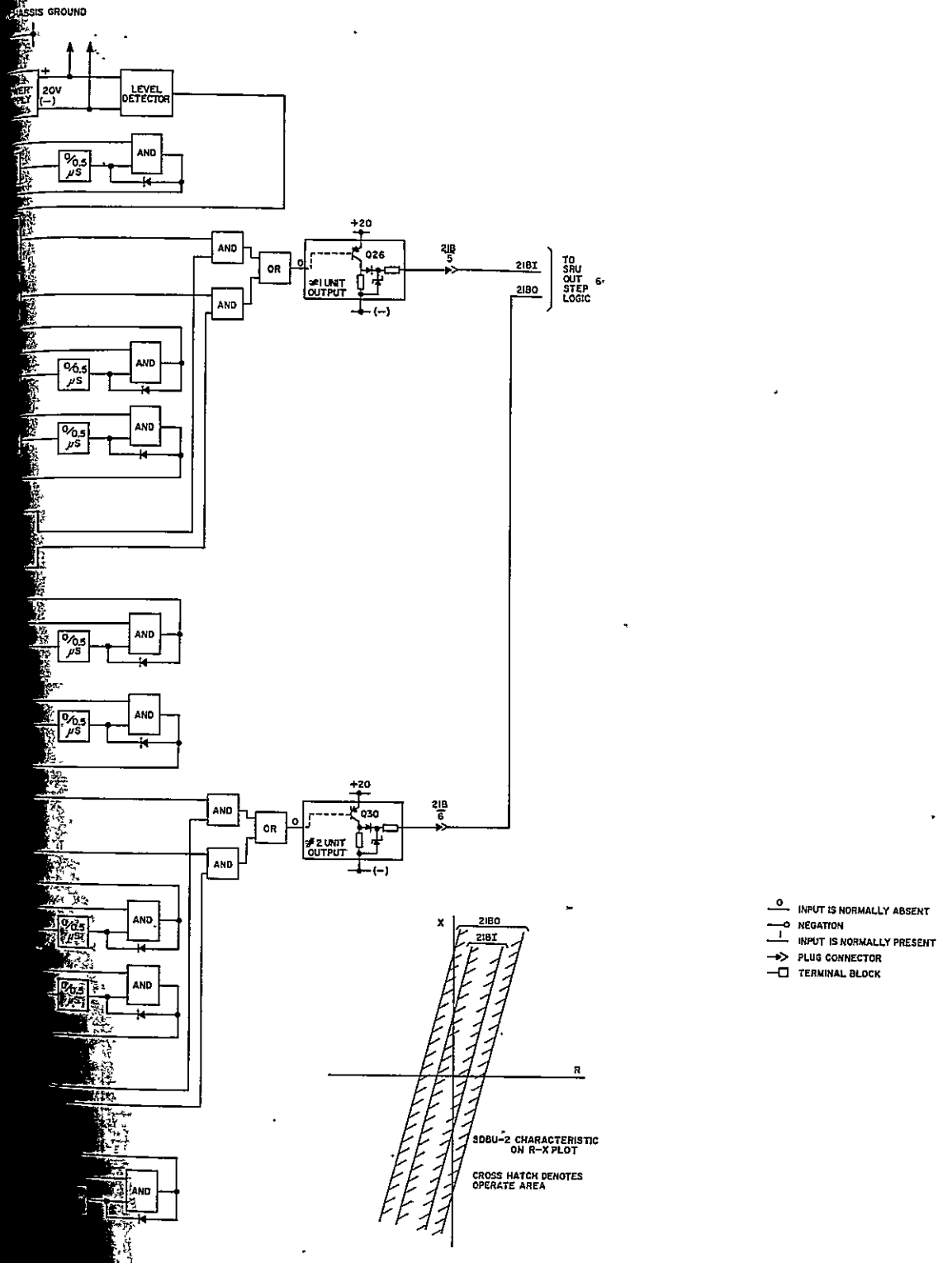


Fig. 8. External Connections of


CHASSIS GROUND
20V (−)
LEVEL DETECTOR
AND
OR
+20
026
#1 UNIT OUTPUT
(−)
2IB 5
2IBI
2IBO
TO SRU OUT STEP LOGIC
030
#2 UNIT OUTPUT
2IB 6
X
R
SDBU-2 CHARACTERISTIC ON R-X PLOT
CROSS HATCH DENOTES OPERATE AREA
INPUT IS NORMALLY ABSENT
NEGATION
INPUT IS NORMALLY PRESENT
PLUG CONNECTOR
TERMINAL BLOCK

5491D45

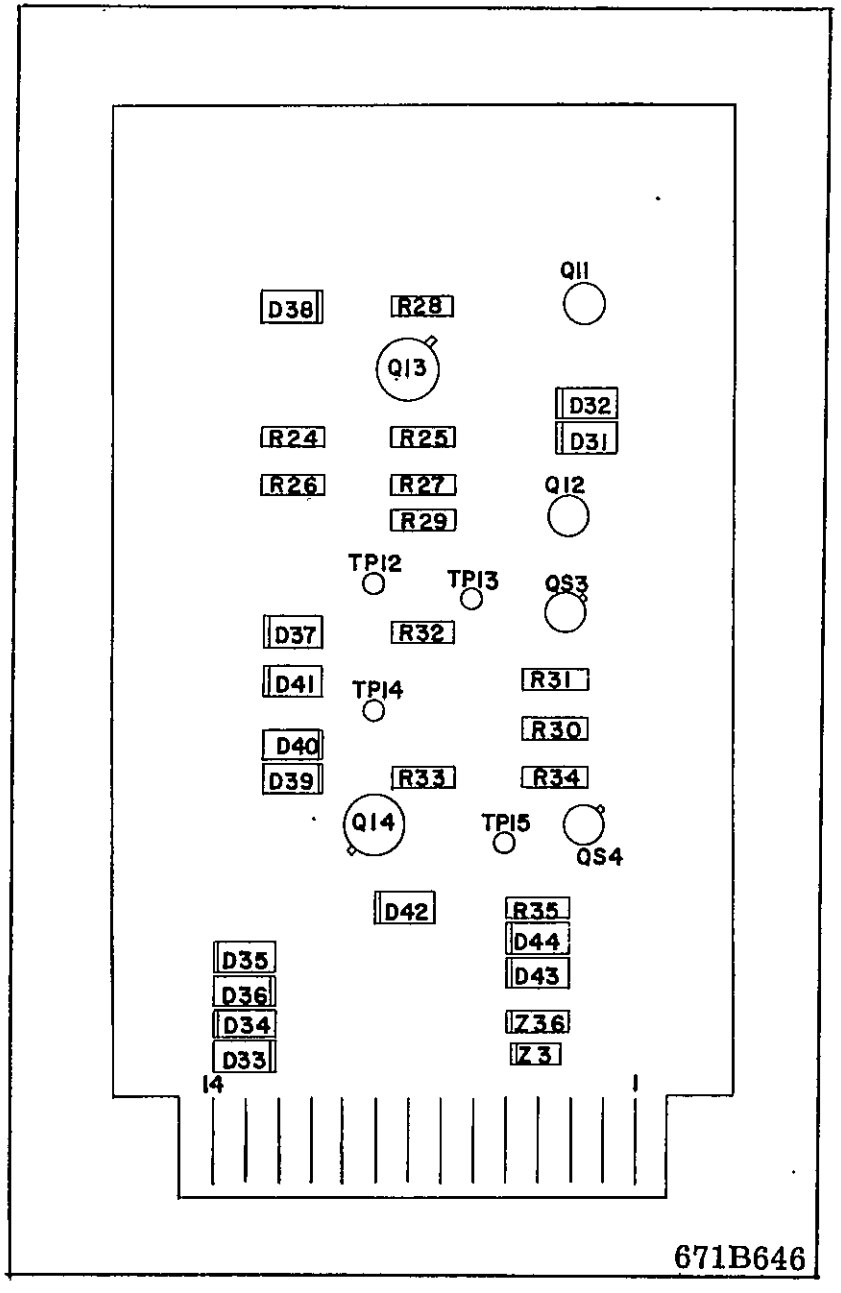


Fig. 11. Polarizing Board "–1"

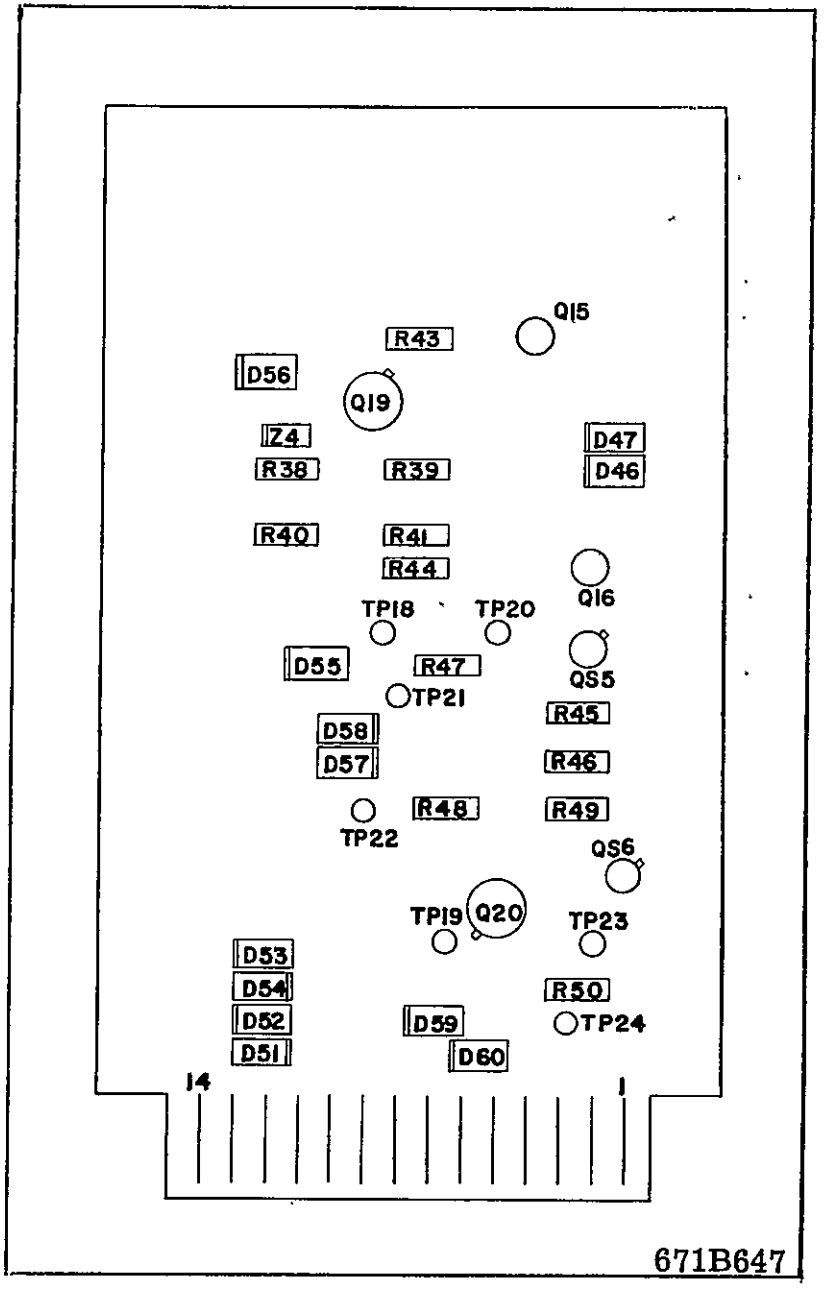


Fig. 12. Polarizing Board "+2"

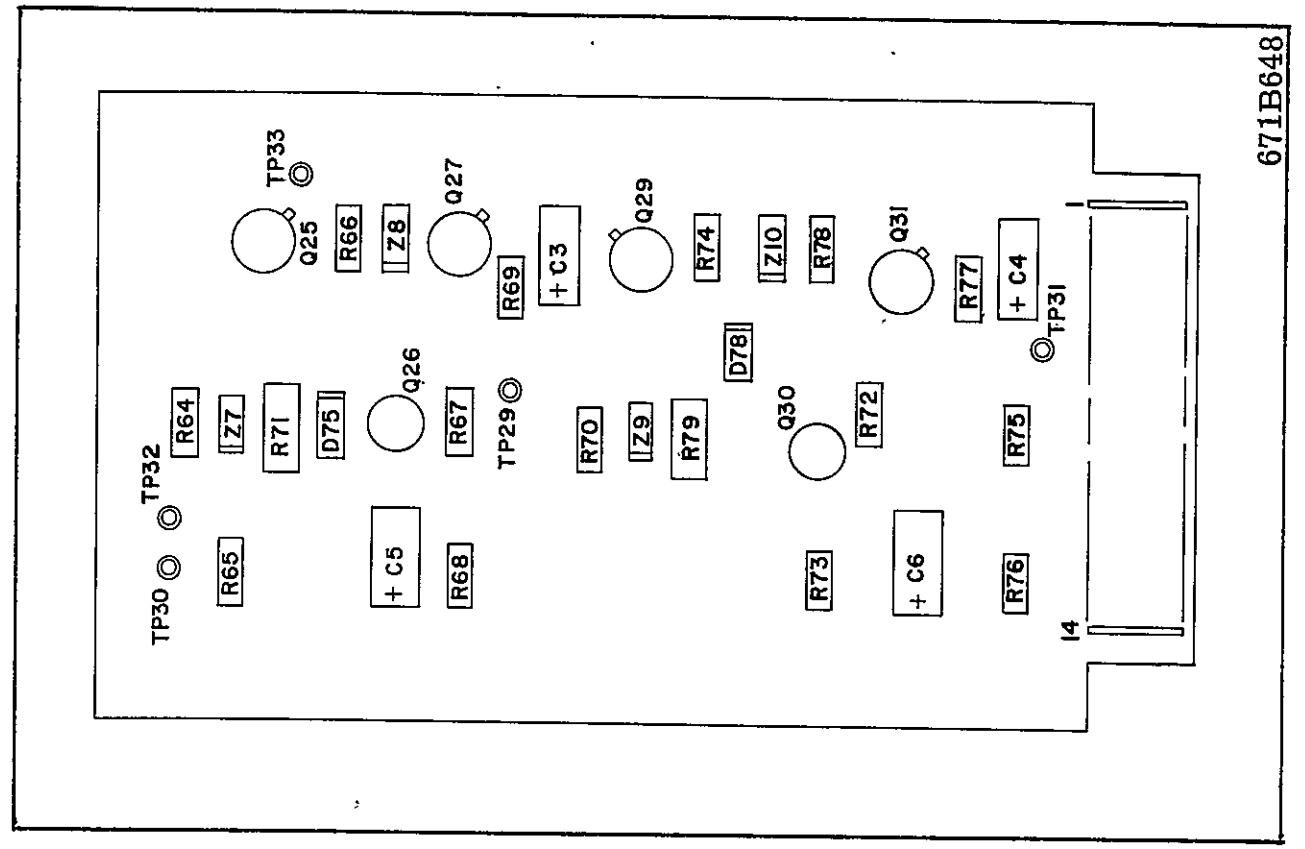


Fig. 14. Output Board

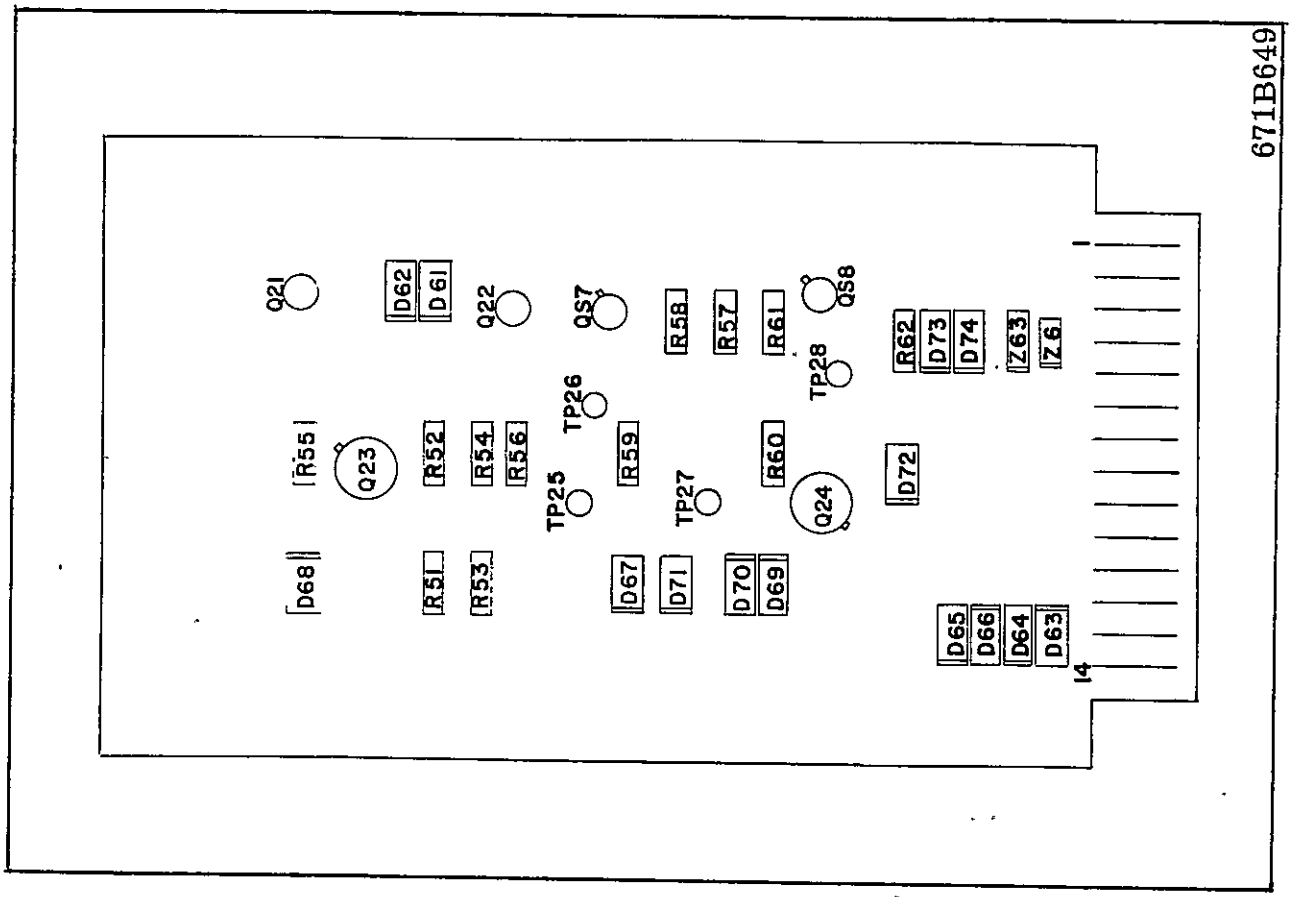


Fig. 13. Polarizing Board "-2"

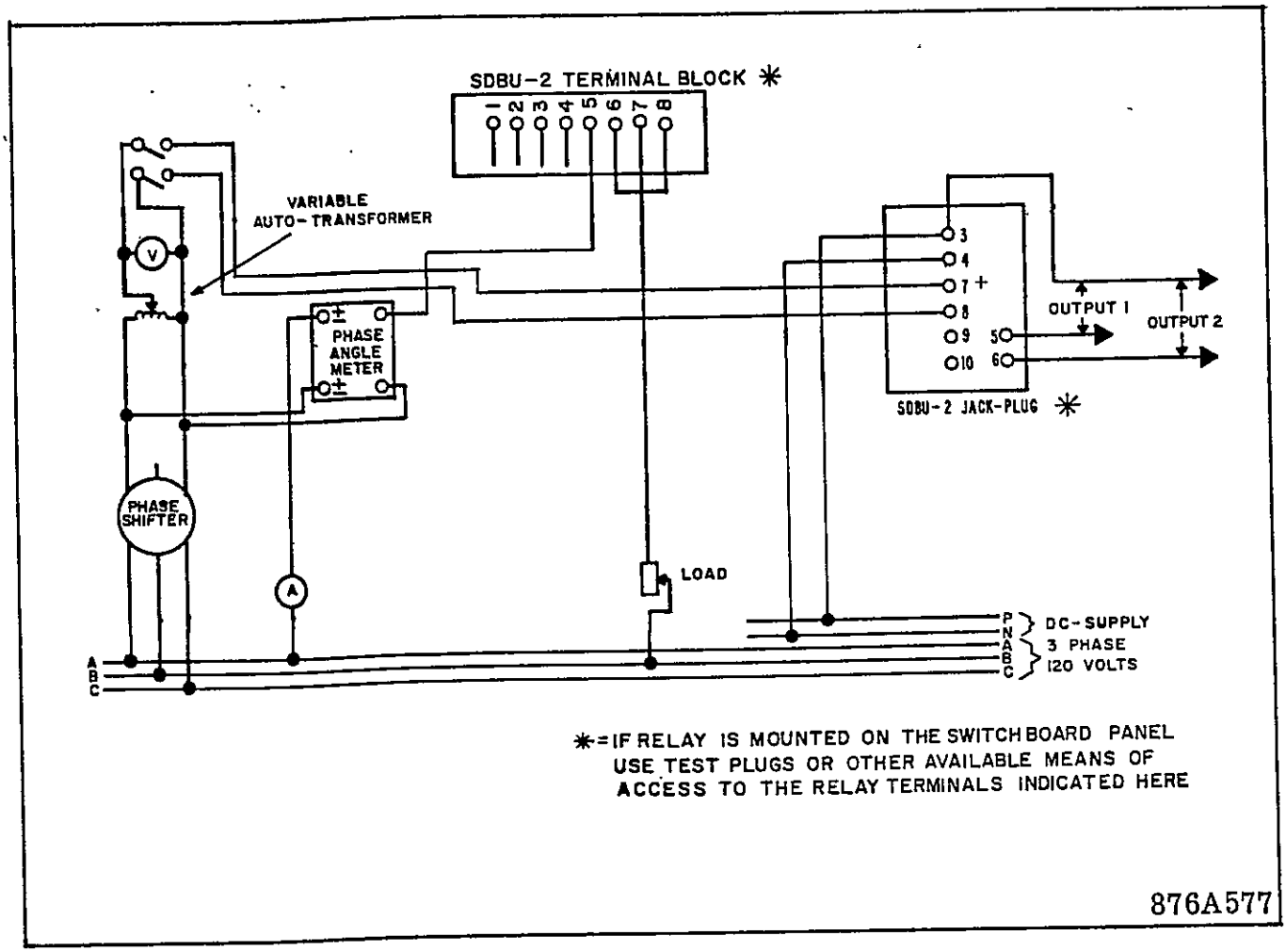


Fig. 15. Test Connections for SDBU-2 Relay

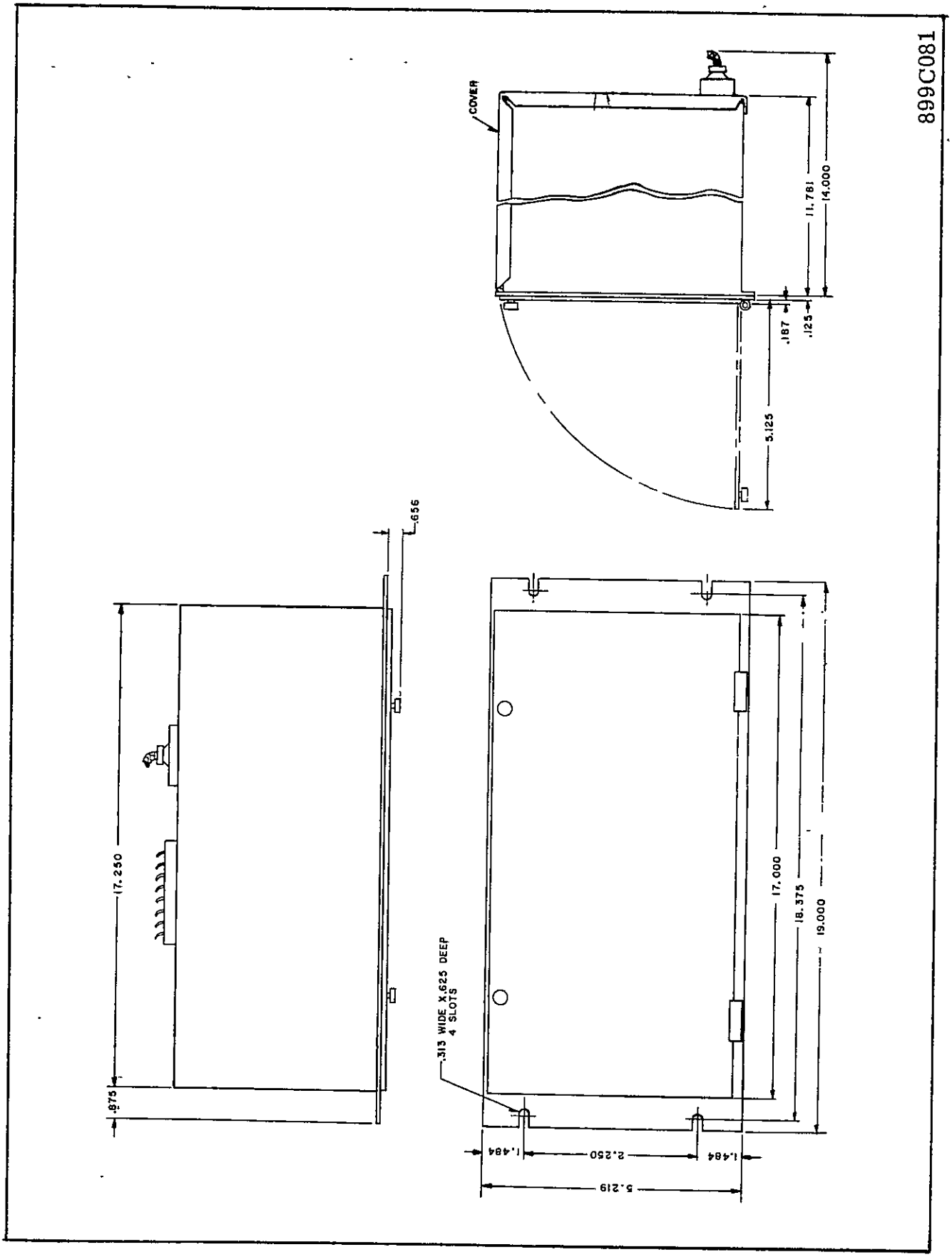


Fig. 16. Case Outline

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.