INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SLB
BREAKER POLE FAILURE RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet, before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. Printed circuit modules should not be removed or inserted while the relay is energized unless specific instructions elsewhere in this instruction leaflet state that such action is permissible. Failure to observe this precaution can result in an undesired tripping output and cause component damage.

APPLICATION

The SLB pole failure relay protects against breaker pole failure, i.e. "pole disagreement". Pole failure is here defined as a pole disagreement (one or more breaker poles open while one or more poles are closed) during non fault conditions.

Types of Breaker Pole Disagreement

1) Pole disagreement during the attempted clearing of a fault. This "breaker failure" condition is detected by conventional breaker failure relay and is cleared by tripping adjacent breakers in normal manner.
2) Pole failure during a breaker closure. This involves the failure of one or more poles to close during a breaker close operation, not involving a fault. This is detected by the SLB current comparison logic which trips the protected breaker after time delay, T2.
3) Pole failure during a breaker opening operation. This involves the failure of one or two poles to interrupt current during a breaker trip operation, not involving a fault. This is detected by the SLB current comparison logic, which calls for another attempt at tripping the protected breaker after delay T2. This attempt will probably not successfully interrupt the stuck pole (s). Therefore, the current comparison logic will continue to operate and ultimately time-out T3 which either operates 86BF to clear the adjacent breakers or alarms the operator.

The SLB outputs are connected as shown in the external schematic diagram, figure 5.

Current Levels and Timing Considerations

As explained in the Operation section of this leaflet, the current comparison logic of the SLB has an output whenever one or more phase (s) carries current above the I_H level (65mA) while one or more phase (s) carries current below the I_L level (20mA). The I_L and I_H settings are factory calibrations, not intended to be changed by the customer.

The I_H level (65mA) is determined as the lowest typical charging current expected on a transmission line. A low level is selected in order to permit the logic to detect a pole disagreement condition during line charging. The I_L level (20mA) is determined by the minimum current level that the relay can reliably detect. Much lower than 20mA will cause the relay to be overly sensitive and subject to pick up on extraneous signals (noise) even though the breaker is open. Of course, the I_L level must not be close to I_H in order to prevent incorrect current comparison outputs due to phase dissymmetries.

A current comparison output condition could occur during a "breaker failure" in which case it is imperative that adjacent breakers be quickly cleared in order to maintain system stability. This is achieved through conventional breaker failure protection which incorporates a timer, device 62, which is set as fast as is required to maintain stability. This is very often a low setting (12 cycles or less) and is sometimes as low as nine cycles. The pole failure timers (T2 and T3) can be set considerably higher than the breaker failure timer, since system stability is not endanagered. A suggested setting for T2 is one second.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

The T3 timer, which either trips adjacent breakers via 86BF or optionally alarms to notify the operator that one of the breaker poles is stuck closed, should be set to coordinate with T2 with a comfortable margin. A suggested setting for T3 is two seconds.

Optional Relay Application – Alarm Only

In some instances it may be desirable to alarm-only for the pole failure condition. This is illustrated in Fig. 5A, the external schematic for the SLB with one timer. A suggested setting for T2 is approximately one second.

CONSTRUCTION & OPERATION

The type SLB relay is a solid state package mounted in FT42 case (See I.L. 41-076); consisting of 3 current to voltage transformers, 3 varistors, 3 sets of full wave rectifiers, 3 filters, 3 sensing circuits, 1 level detector, and a standard output circuit. It contains a 20-volt zener supply that energizes the relay logic. It also self-contains one or two timers (of same design as (W) Type TD-50 relays) for adjustable time delay applications. All 3 transformers, TA, TB, TC have a center-tapped secondary which is tied together with the DC negative for a common ground. Transformer's secondaries are connected to individual varistors to keep the secondary voltages at a safe level.

There are 2 sets of full wave rectifiers for each phase. The odd numbered diodes are used to rectify the quantities related to the I_H or high current. These quantities will be compared to a reference at the level detector. The even numbered diodes rectify quantities that will provide a signal for phase current detection. Rectified quantities are then filtered by a capacitor and the input to the current sensors is then kept at a safe value by means of zener diodes.

The level detector is adjusted to provide a 20-volt output whenever one or more phase current is equal or greater than 65mA. This output can then drive the relay output circuit and produce an output if at least one of the phase currents drops below 20mA as detected by the related current sensing circuit. The basic current sensing circuit consists of a transistor that is biased into a normally on condition for a phase current equal or greater than 20mA. If any phase current drops below 20mA the related transistor (Q1, Q2, or Q3) will turn off allowing any output from the level detector to deliver power to the output circuit and thus producing a relay output.

The level detector output is delayed by about 15 ms to avoid undesired tripping due to normal breaker unsymmetries. This delay circuit consists of an R-C timer, a zener diode and an output transistor. The output of this timer is used as the B+ supply for the current sensing circuits. Figures 5, 6, and 7 show some of the basic circuits described above. Relay produces telephone relay output which is delayed by means of time delay logic (self-contained timers equivalent to TD-50 relay). Standard time delay ranges are .05 to 1.0 sec. and .2 to 4 sec. For detailed characteristics of the timers refer to TD-50 relay information, (W) L-779641 and I.L. 41-579.1.

CHARACTERISTICS

A. Current Rating

Continuous	5 Amperes, 3 ϕ
One Second	100 Amperes, 3 ϕ

B. Operating Time *

Maximum	30 MS
Minimum	15 MS

*Plus timer setting

C. DC Supply

Current Burden Per Phase

90 MA	.05 VA
5 A	11.5 VA

D. DC Burden

No timer	0.07 Amps.
One timer – 48 VDC	0.25 Amps.
Two timer – 48 VDC	0.5 Amps.
One timer – 125 VDC	.195 Amps.
Two timer – 125 VDC	.380 Amps.

E. Tripping Condition

At least one phase conducting 0.065 ampere or more while at least one phase is conducting less than 0.018 ampere.

F. Restraining Conditions

1) Sudden increase of current from 0.0 ampere to any value greater than 0.065 ampere in all phases, whether balanced or not.

2) Any sudden change in current, increase or decrease, balanced or not, as long as the minimum current is greater than 0.065 ampere in all three phases.

3) Simultaneous interruption of all three currents, balanced or not.

G. Settings

Proper time delay is selected by turning the knob of potentiometers R47 and R50 (dialed).

External Connections

Fig. 4 shows the external connections for the type SLB relay.

Receiving Acceptance

Make a visual inspection to make sure that there are no loose connections, broken resistors, or broken resistor wires.

Check relay per following procedure:

A. Refer to figure 10 in this I.L.

B. Connect per test figure and apply rated DC voltage.

C. Apply I_A = 15mA, $I_B = I_C$ = 100mA. A 20 volt output should be observed at logic PCB terminal #19, and telephone relay TR2 (and TR3 for 2 timer relays) should operate.

D. Apply I_B = 15mA, $I_A = I_C$ = 100mA, and check relay output per step C.

E. Apply I_C = 15mA, $I_A = I_B$ = 100mA, and check relay output per part C.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from moisture. Mount the relay by means of the four mounting holes on the flange for semi-flush mounting or by means of the rear mounting stud or studs for projection mounting. Either a mounting stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel-panel mounting or to the terminal studs furnished with the relay for thick panel mounting. The terminal studs may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench. For detailed FT case information, refer to I.L. 41-076.

Routine Maintenance

All relays should be checked at least once every year or at such time intervals as may be dictated by experience to be suitable to the particular application.

Calibration – Refer to Fig. 10

Use the following procedure for calibrating the relay if the relay adjustments have been adjusted or disturbed. This procedure should not be used unless it is apparent the relay is not in proper working order.

A. Level Detector

1. Energize relay with rated DC voltage.
2. Apply I_A = 65mA, $I_B = I_C = 0$
3. Monitor relay output (PCB TP19 – top left) and adjust R45 (trim-pot – same board) until relay output (full output) is just observed.
4. Reduce I_A to about 63mA and adjust R46 (same board – top right), until output drops to zero.
5. Increase I_A and relay output should be observed as current reaches 65mA.
6. Reduce I_A and recheck per step 4.
7. In general adjust R45 for pickup, and R46 for drop out until relay produces an output (full output) as current approaches 65mA and drops out quickly if current is, then, reduced.

B. Current Sensors (fig. 10)

1. Apply rated DC voltage.
2. Apply I_A = 20mA, $I_B = I_C$ = 1 Amp. Monitor relay output (TP9, by PCB).
3. Adjust R39 (circuit board – bottom left) until the first output indication (or first meter deflection), is just observed. If relay was already picked up, adjust R39 until it drops out, and then adjust it again as specified above.
4. Reduce current I_A, observing the relay output. Complete relay output (Vo = 20) should be observed within 3mA. Recheck first output indication at 20mA.
5. Adjust R40 (bottom – center) per steps 3 and 4, this time setting $I_A = I_C$ = 1 Amp, I_B = 20mA.

NOTE: Output telephone relays should also operate everytime full trip was indicated by TP9 (PCB – logic), for duration of timer setting(s).

Renewal Parts

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data.

References

FT case	I.L. 41-076
TD-5 Timer	I.L. 41-579.1
TD-50 Timer	L-779641

PARTS LIST

Part Name	(W) Style or Reference
1. Transformer (T_A, T_B, T_C)	290B300G01
2. Varistor (VR1, VR2, VR3)	183A122H01
3. Zener (20V, 10W)	762A631H01
4. DC Resistor 48V	1202587
125V	1267293
250V	1202954
5. Printed Circuit Board Logic	6294D37G01
6. Printed Circuit Board Timer	205C548G01

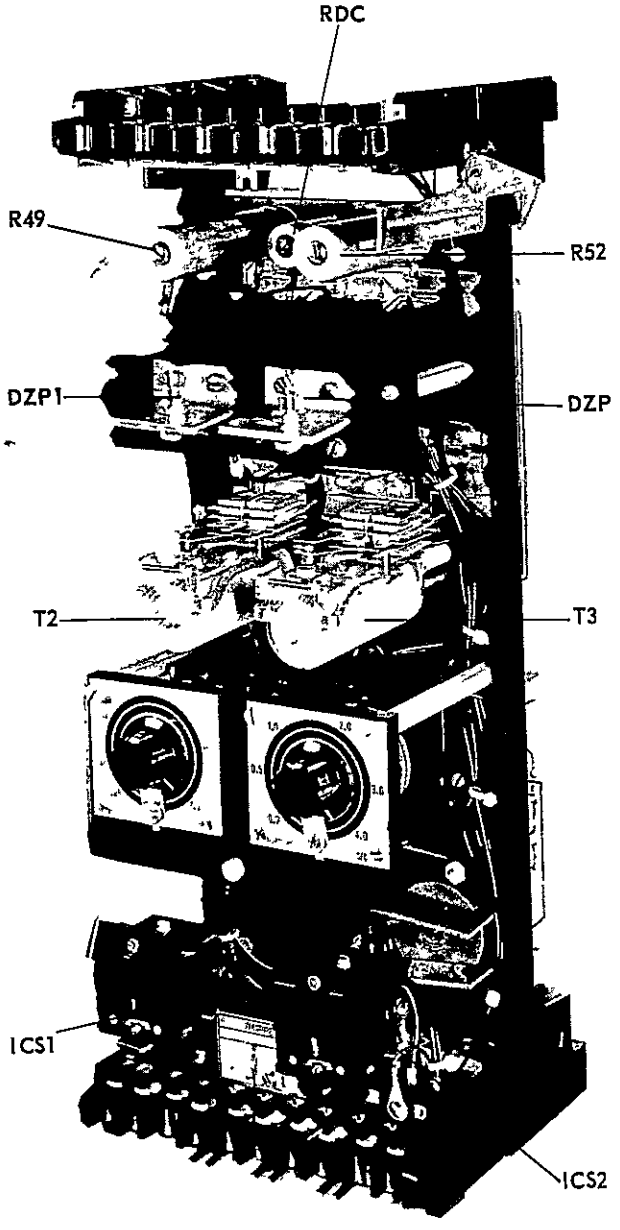


Fig. 1 Relay Picture.

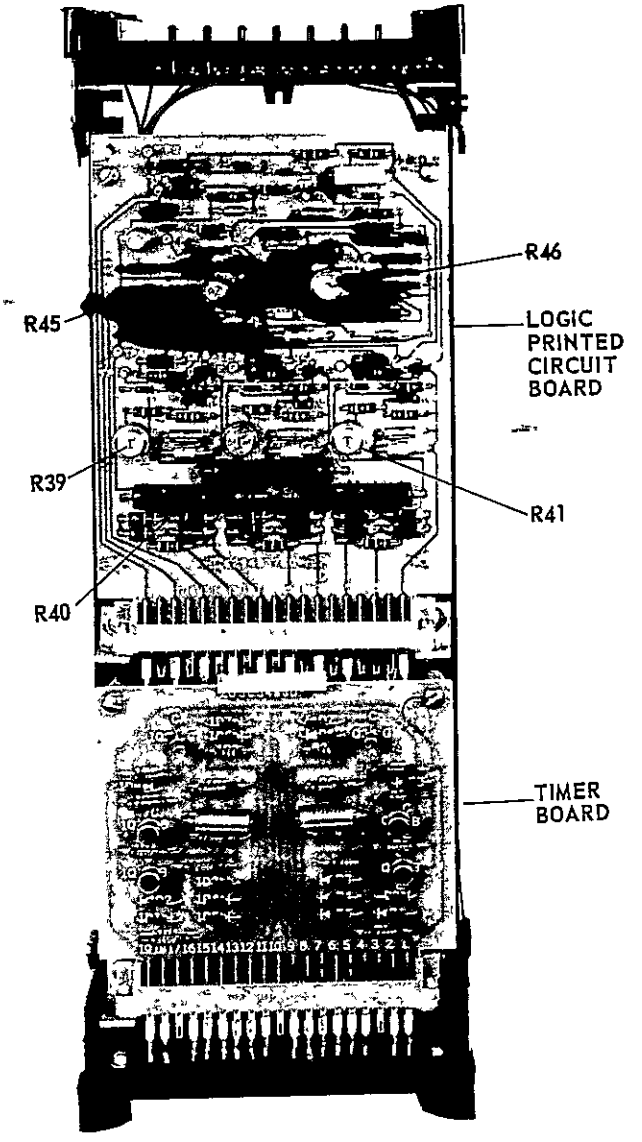


Fig. 2 Relay Picture

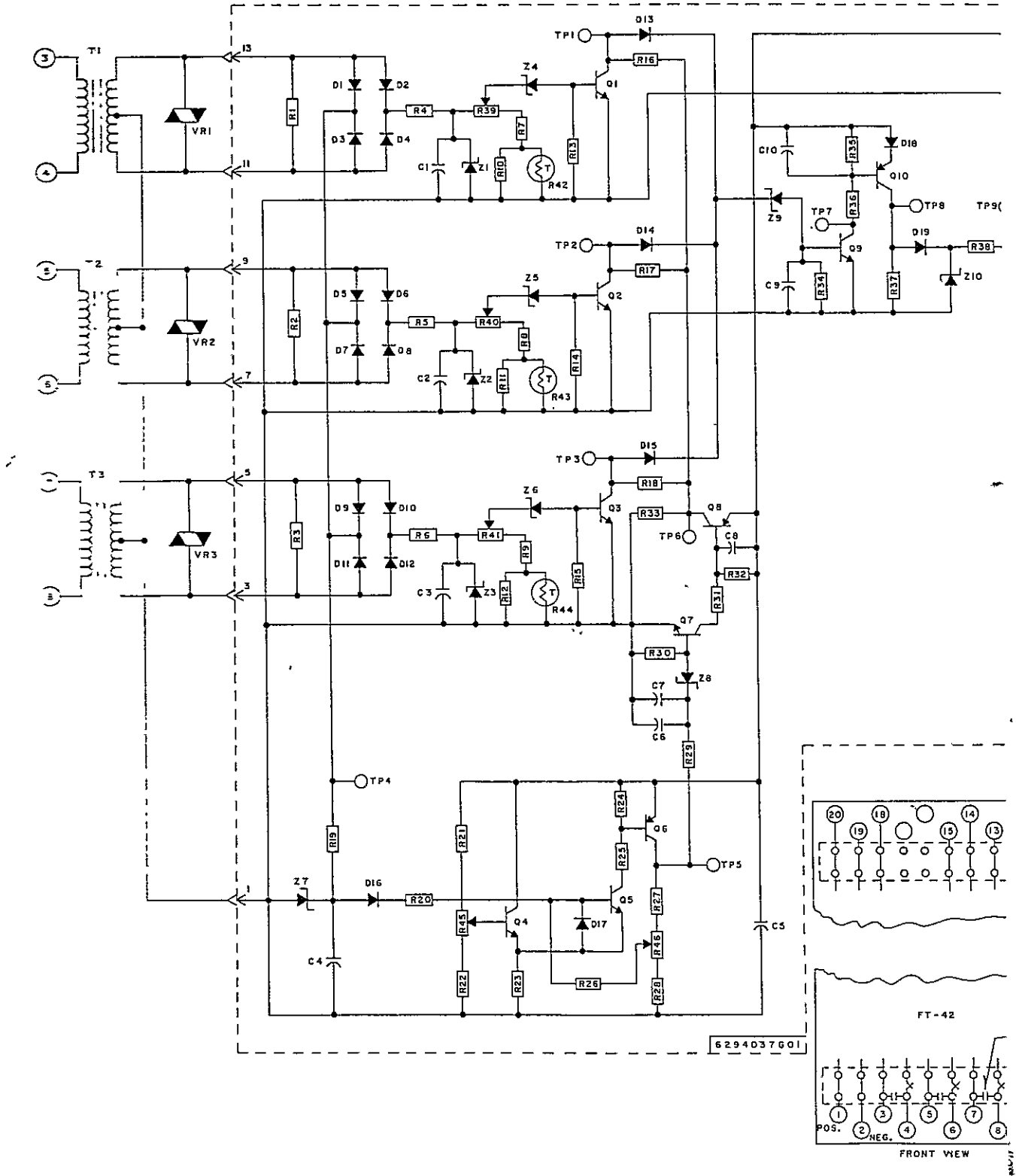
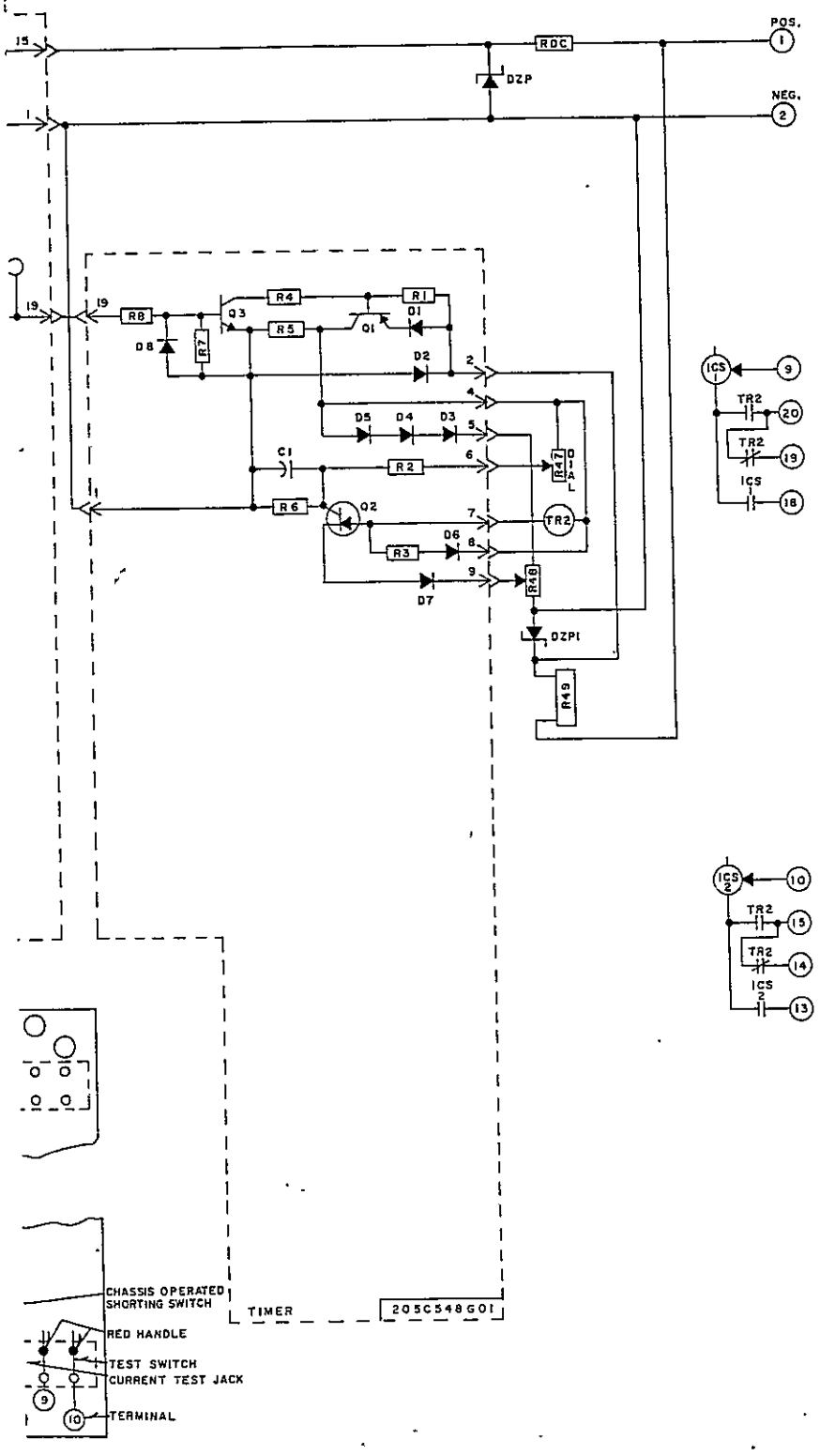


Fig. 3 Internal-Sc



	CAPACITOR	STYLE	REQ.	REF.
	C1	187A508H04	1	39 MFD.
	DIODE			
	D1-D8	184A855H13	8	IN645
	TRANSISTOR			
	Q1	184A638H20	1	2N1132
	Q2	185A517H03	1	2N886
	Q3	184A638H18	1	2N697
	RESISTOR			
*	R2	862A376H01	1	1K -1/2W- ±1%
	R1-R5	836A503H42	2	4,990Ω-1/2W- ±1%
•	R2	184A764H21	1	562Ω -1/2W- ±1%
	R3	184A763H13	1	270Ω -1/2W- ±5%
	R4	836A503H30	1	1,500Ω-1/2W- ±1%
•	R6	862A377H77	1	61.9K -1/2W- ±1%
	R7	836A503H34	1	2,210Ω-1/2W- ±1%
	R8	836A503H53	1	15K -1/2W- ±1%
*	R6	862A377H77	1	61.9K -1/2W- ±1%
	CAPACITOR			
	C1-C2-C3	862A530H01	3	.33 MFD.
	C4	837A241H02	1	.01 MFD.
	C5	187A508H10	1	18 MFD.
	C6-C8-C10	837A241H03	3	.27 MFD.
	C7	837A241H16	1	2.2 MFD.
	C9	876A409H01	1	.18 MFD.
	DIODE			
	D1 TO D12	188A342H11	12	IN4822
	D13-D14-D15-D18	188A342H06	4	IN4818
	D16-D17	184A855H14	2	IN4385
	D19	837A692H03	1	IN645A
	TRANSFORMER			
	T1-T2-T3	2908300G01	3	
	TRANSISTOR			
	Q1-Q2-Q3-Q5-Q7-Q9	848A851H02	6	2N3417
	Q4	184A638H18	1	2N697
	Q6	184A638H20	1	2N1132
	Q8-Q10	849A441H01	2	2N3645
	RESISTOR			
	R1-R2-R3	184A763H62	3	30K -1/2W- ± 5%
	R4-R5-R6-R19	837A237H21	4	1200Ω-1W- ± 5%
	R7-R8-R9-R25-R29-R32	184A763H47	6	6.8K -1/2W- ± 5%
	R10-R11-R12	184A763H71	3	68K -1/2W- ± 5%
	R13-R14-R15-R24 R30-R31-R34	184A763H51	7	10K -1/2W- ± 5%
	R16-R17-R18-R35	184A763H59	4	22K -1/2W- ± 5%
	R20	184A763H61	1	27K -1/2W- ± 5%
	R21-R22	184A763H35	2	2.2K -1/2W- ± 5%
	R23-R36	184A763H43	2	4.7K -1/2W- ± 5%
	R26-R33-R37	184A763H73	3	82K -1/2W- ± 5%
	R27	184A763H53	1	12K -1/2W- ± 5%
	R38	762A679H01	1	150Ω-3W
	R39-R40-R41-R46	629A430H01	4	50K -1/4W- ± 20%
	R42-R43-R44	185A211H01	3	53,800Ω - ±10%
	R45	862A406H02	1	20K - .5W - ±10%
	R47	184A756H04	1	20K
	R48	185A067H05	1	250Ω
	R49 (125 VDC)	1336173	1	360Ω-40W- ± 5%
	R49 (48 VDC)	040I299H66	1	95Ω-40W- ± 5%
	ZENER DIODE			
	Z1-Z2-Z3	188A302H03	3	IN3016
	Z4-Z5-Z6-Z9	186A797H13	4	IN748A
	Z7-Z8	188A302H17	2	IN3021B
	Z10	862A288H01	1	IN3688A
	DZP	762A631H01	1	IN2984B
	DZP1	629A798H03	1	IN2986B
	VARISTOR			
	VR1-VR2-VR3	183A122H02	3	12K - ±20%
	TELEPHONE RELAY			
	TR2	407C614H06	1	
	RESISTOR			
	RDC (125 VDC)	1267293	1	1.5K - 25W - ± 5%
	RDC (48 VDC)	1202587	1	400Ω-25W- ± 5%

• = SPECIAL .02 TO .2 SEC. TIMER.
* = FOR .05 TO 1 SEC. TIMER.

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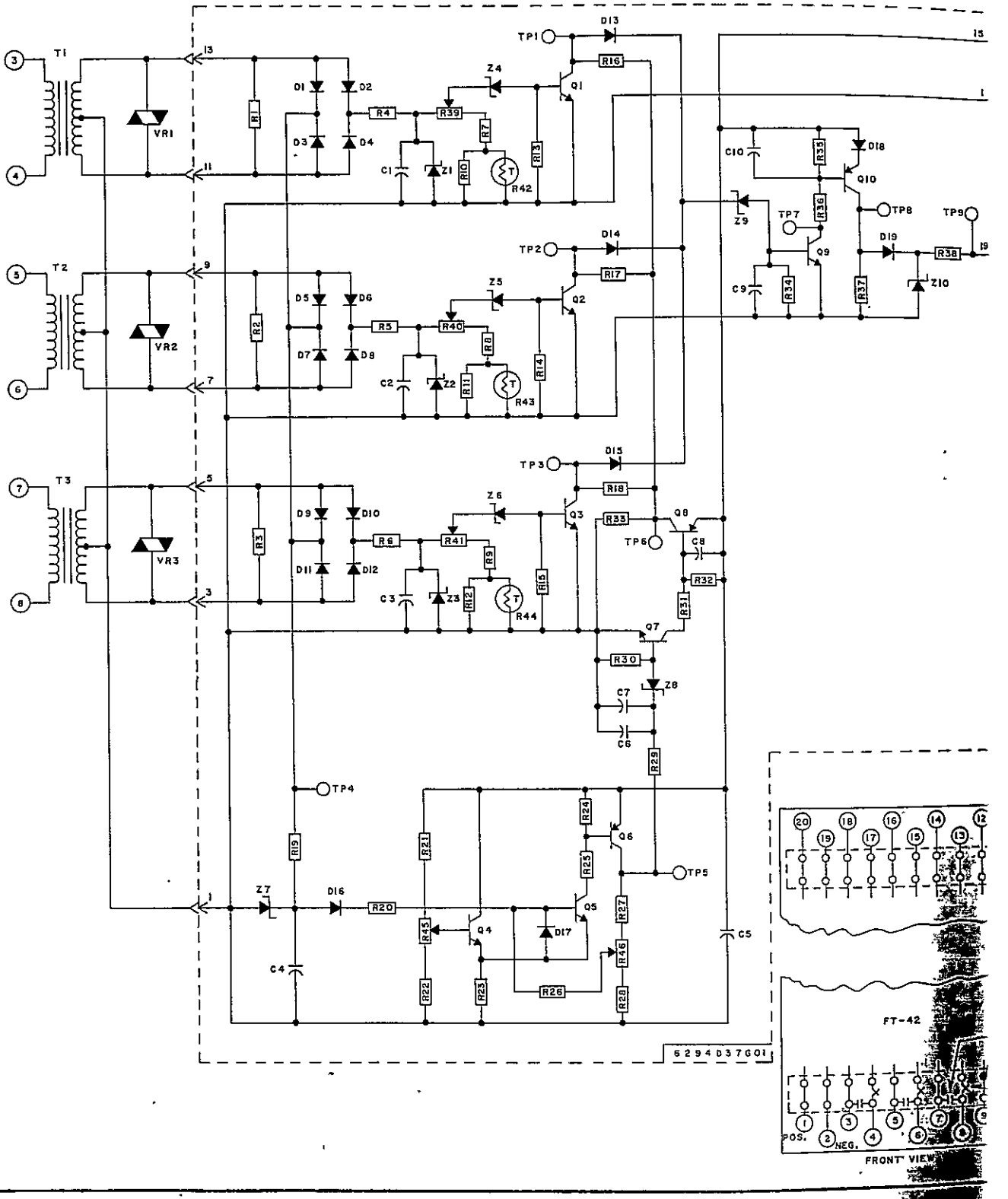
hematic (1 Timer)


T1
T2
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VR1
VR2
VR3
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
Q1
Q2
Q3
Q4
Q5
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R45
R46
C1
C2
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C4
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C7
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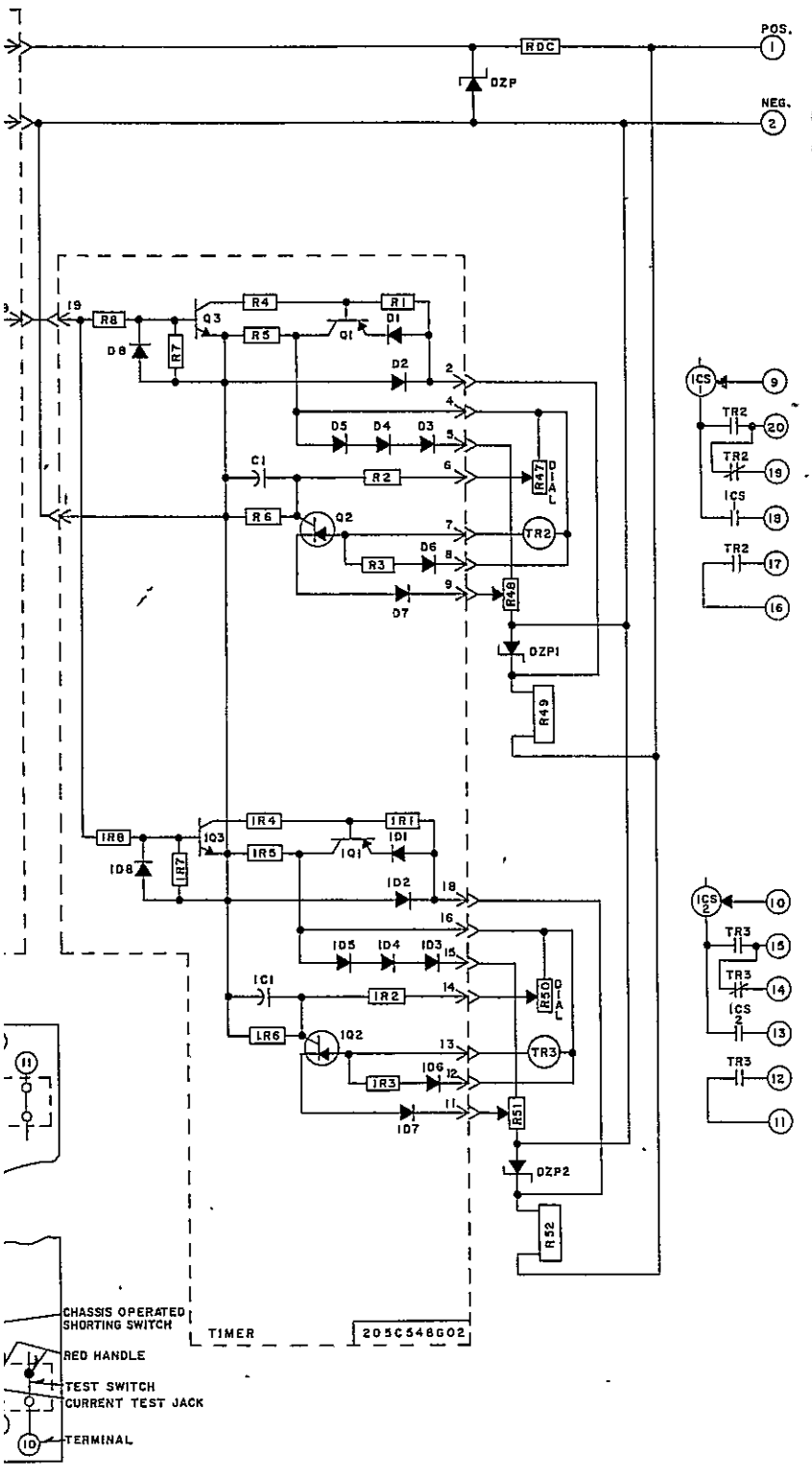
C9
C10
5294037G01
FT-42
POS.
NEG.
FRONT VIEW

Fig 4 Inter

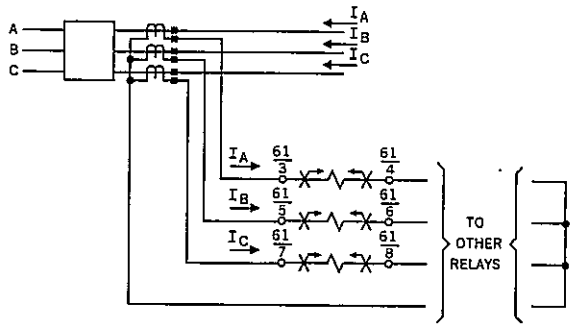


CAPACITOR	STYLE	REQ.	REF.
C1 - IC1	187A508H04	2	39 MFD.
DIODE			
D1 TO D8 - ID1 TO ID8	184A855H13	16	IN645
TRANSISTOR			
Q1 - IQ1	184A638H20	2	2N1132
Q2 - IQ2	185A517H03	2	2N886
Q3 - IQ3	184A638H18	2	2N697
RESISTOR			
* R2	862A376H01	1	1K -1/2W- ±1%
R1-R5-IR1-IR5	836A503H42	4	4,990Ω-1/2W- ±1%
● IR2	862A376H73	1	5.62K -1/2W- ±1%
R3-IR3	184A763H13	2	270Ω-1/2W-±5%
R4-IR4	836A503H30	2	1,300Ω-1/2W-±1%
* R6	862A377H77	1	61.9K -1/2W-±1%
R7-IR7	836A503H34	2	2,210Ω-1/2W-±1%
R8-IR8	836A503H53	2	15K -1/2W-±1%
● IR6	862A378H42	1	267K -1/2W-±1%
CAPACITOR			
C1-C2-C3	862A530H01	3	33 MFD.
C4	837A241H02	1	0.1 MFD.
C5	187A508H10	1	18 MFD.
C6-C8-C10	837A241H03	3	.27 MFD.
C7	837A241H16	1	2.2MFD.
C9	876A409H01	1	.18 MFD.
DIODE			
D1 TO D12	188A342H11	12	IN4822
D13-D14-D15-D18	188A342H06	4	IN4818
D16-D17	184A855H14	2	IN4385
D19	837A692H03	1	IN645A
TRANSFORMER			
T1-T2-T3	29083006G01	3	
TRANSISTOR			
Q1-Q2-Q3-Q5-Q7-Q9	848A851H02	6	2N3417
Q4	184A638H18	1	2N697
Q6	184A638H20	1	2N1132
Q8-Q10	849A441H01	2	2N3645
RESISTOR			
R1-R2-R3	184A763H62	3	30K -1/2W- ± 5%
R4-R5-R6-R19	837A237H21	4	1200Ω-1W- ± 5%
R7-R8-R9-R25-R29-R32	184A763H47	6	6.8K -1/2W- ± 5%
R10-R11-R12	184A763H71	3	68K -1/2W- ± 5%
R13-R14-R15-R24 R30-R31-R34	184A763H51	7	10K -1/2W- ± 5%
R16-R17-R18-R35	184A763H59	4	22K -1/2W- ± 5%
R20	184A763H61	1	27K -1/2W- ± 5%
R21-R22	184A763H35	2	2.2K -1/2W- ± 5%
R23-R36	184A763H43	2	4.7K -1/2W- ± 5%
R26-R33-R37	184A763H73	3	82K -1/2W- ± 5%
R27	184A763H53	1	12K -1/2W- ± 5%
R38	762A679H01	1	150Ω- 3W
R39-R40-R41-R46	629A430H01	4	50K -1/4W- ± 20%
R42-R43-R44	185A211H01	3	53,800Ω - ±10%
R45	862A406H02	1	20K - .5W - ±10%
R47 - R50	184A756H04	2	20K
R48 - R51	185A067H05	2	250Ω
R49 - R52 (125 VDC)	1336173	2	560Ω-40W- ± 5%
R49 - R52 (48 VDC)	04D1299H66	2	95Ω-40W- ± 5%
ZENER DIODE			
Z1 - Z2 - Z3	188A302H03	3	IN3016
Z4 - Z5 - Z6 - Z9	186A797H13	4	IN748A
Z7 - Z8	188A302H17	2	IN3021B
Z10	862A286H01	1	IN3688A
DZP	762A631H01	1	IN2984B
DZP1 - DZP2	629A798H03	2	IN2986B
VARSISTOR			
VR1 - VR2 - VR3	183A122H02	3	12K - ±20%
TELEPHONE RELAY			
TR2 - TR3	407C614H06	2	
RESISTOR			
RDC (125VDC)	1267293	1	1.5K - 25W - ± 5%
RDC (48 VDC)	1202587	1	400Ω-25W- ± 5%

*= FOR .05 TO 1 SEC. TIMER.
●= FOR .2 TO 4 SEC. TIMER.

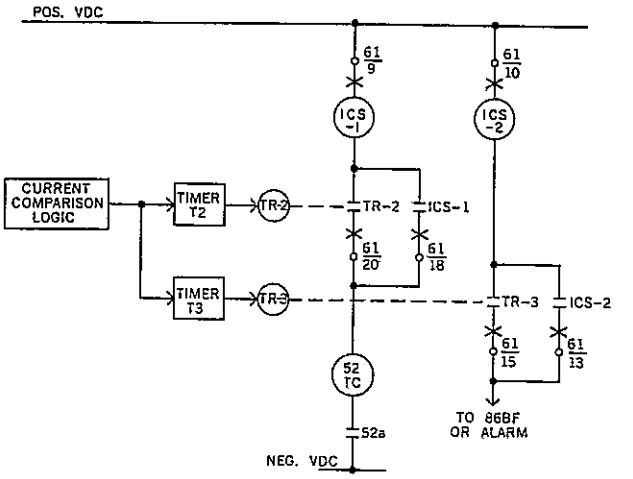
6295D51

ıal Schematic (2 Timer)



DEVICE NUMBER CHART

61 – POLE FAILURF RELAY, TYPE SLB, WITH TWO TIMERS
86BF – BREAKER FAILURE LOCK–OUT RELAY.
52 – POWER CIRCUIT BREAKER.
ICS – INDICATING CONTACTOR SWITCH.



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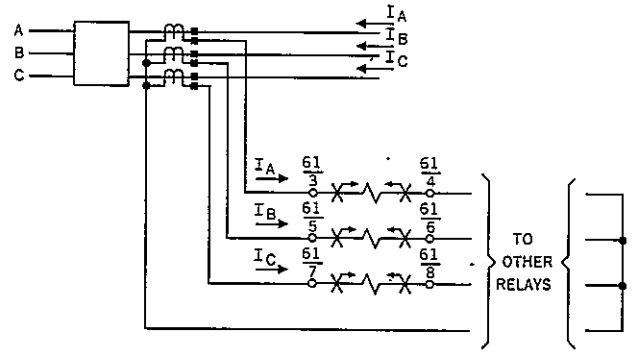
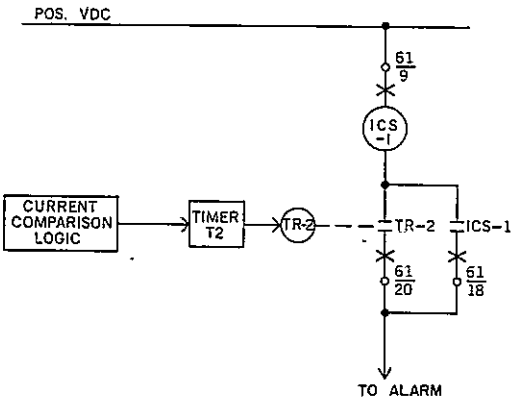


DEVICE NUMBER CHART

61 – POLE FAILURF RELAY, TYPE SLB, WITH ONE TIMER.
86BF – BREAKER FAILURE LOCK–OUT RELAY.
52 – POWER CIRCUIT BREAKER.
ICS – INDICATING CONTACTOR SWITCH.



719B481

Fig. 5 External Connections (1 Timer) (2 Timers)

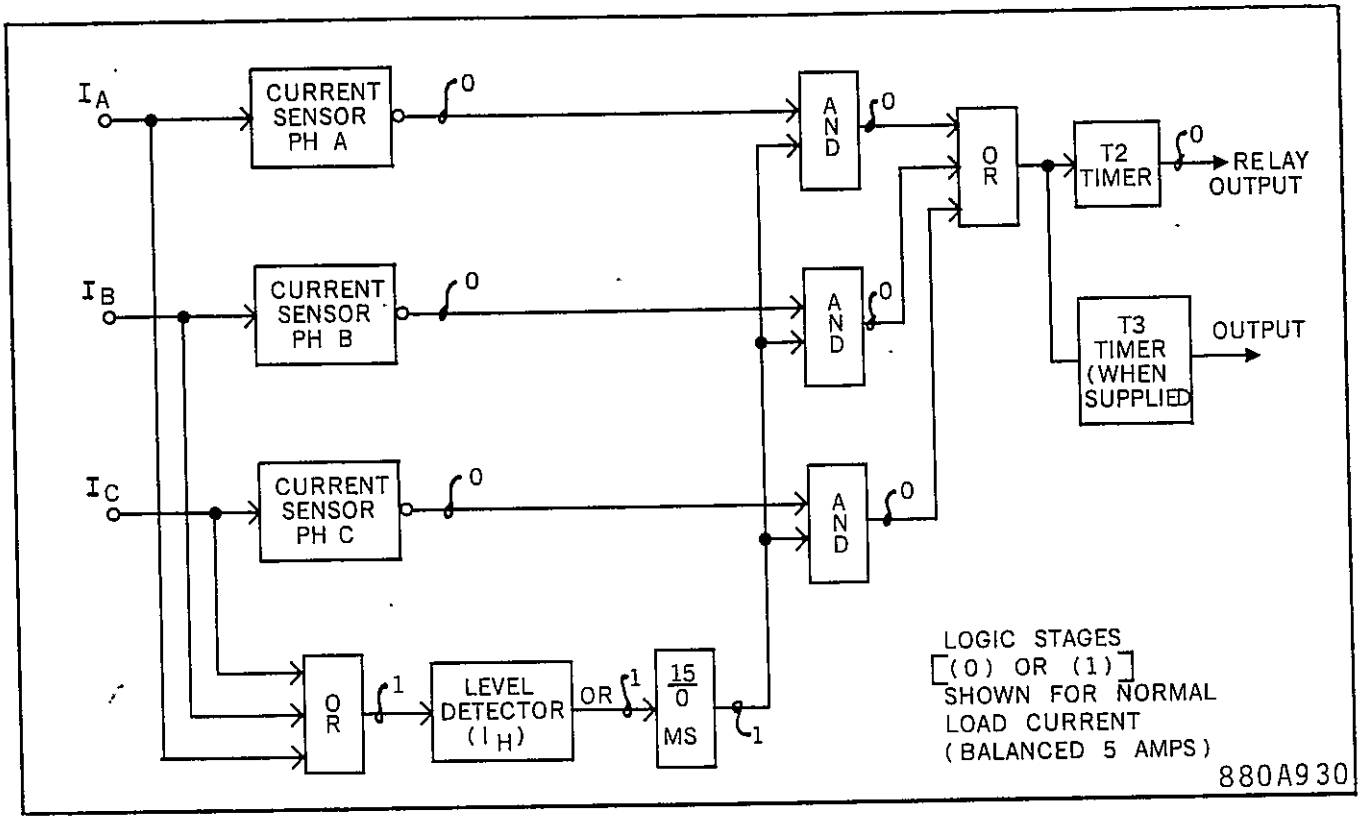


Fig. 6 Logic Block Diagram

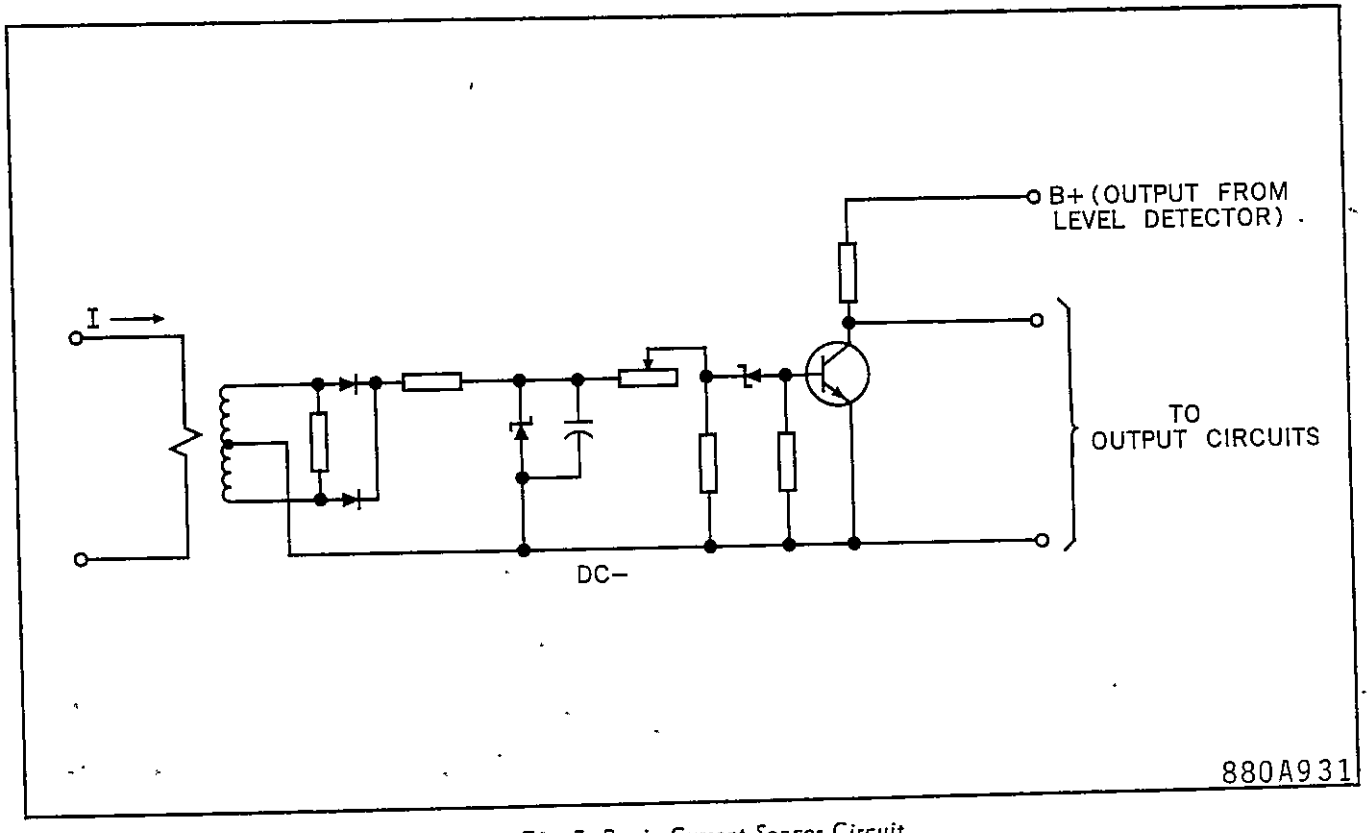


Fig. 7 Basic Current Sensor Circuit

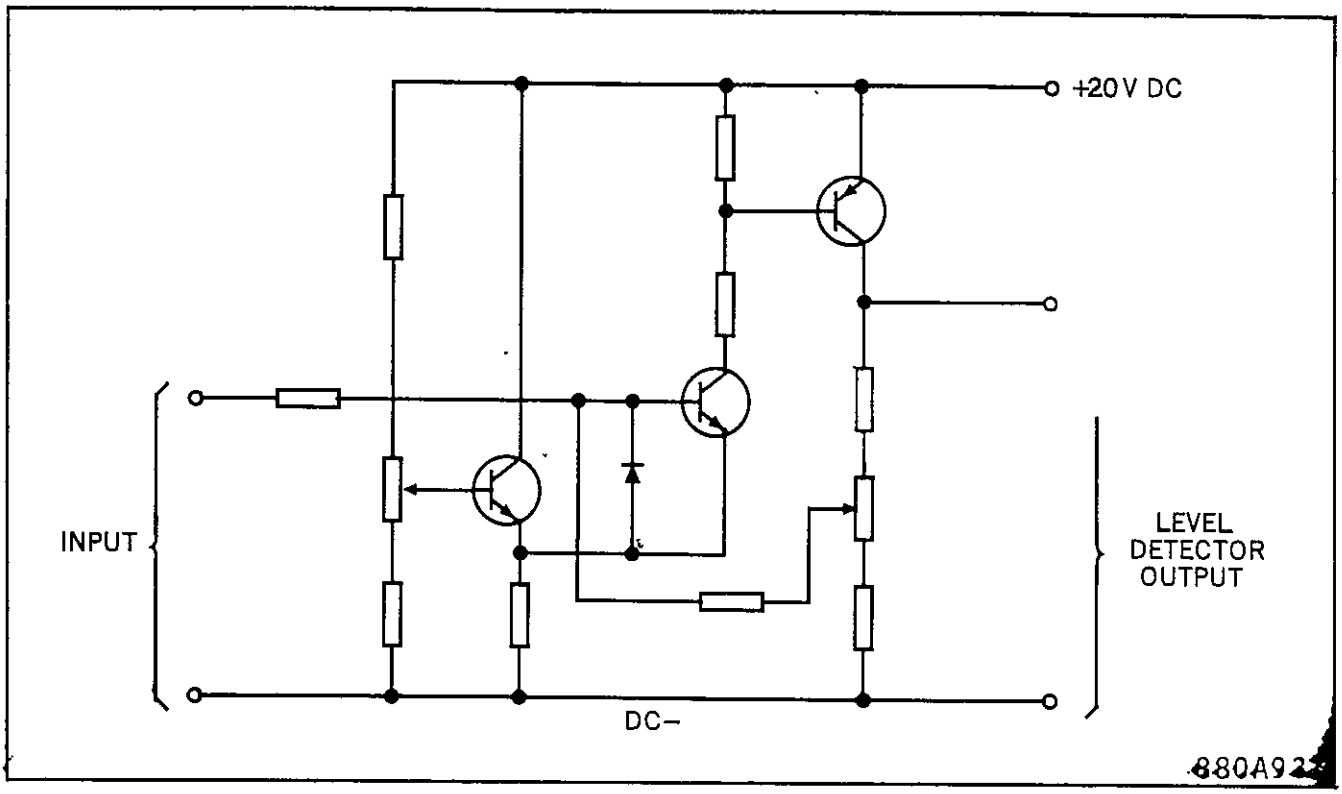


Fig. 8 Level Detector

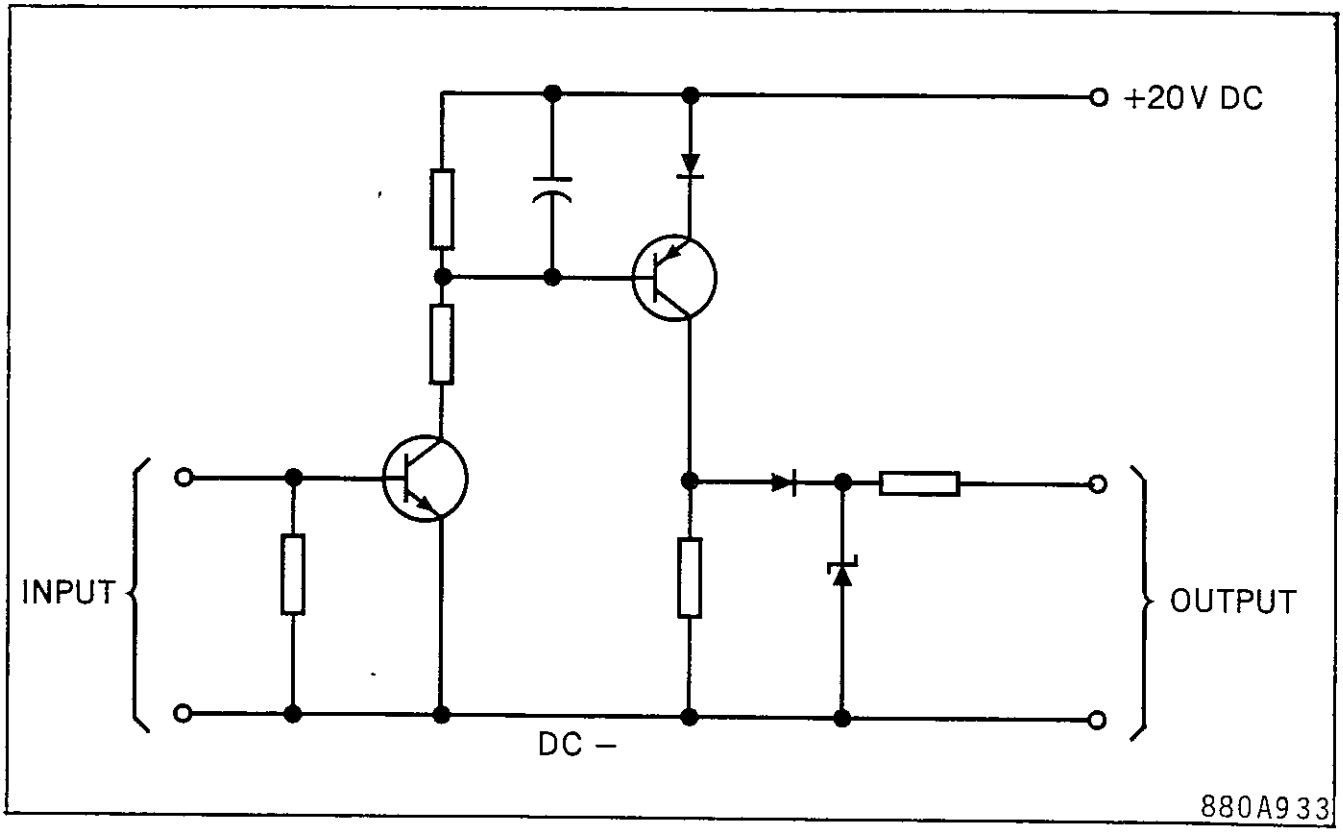


Fig. 9 Standard Output Circuit

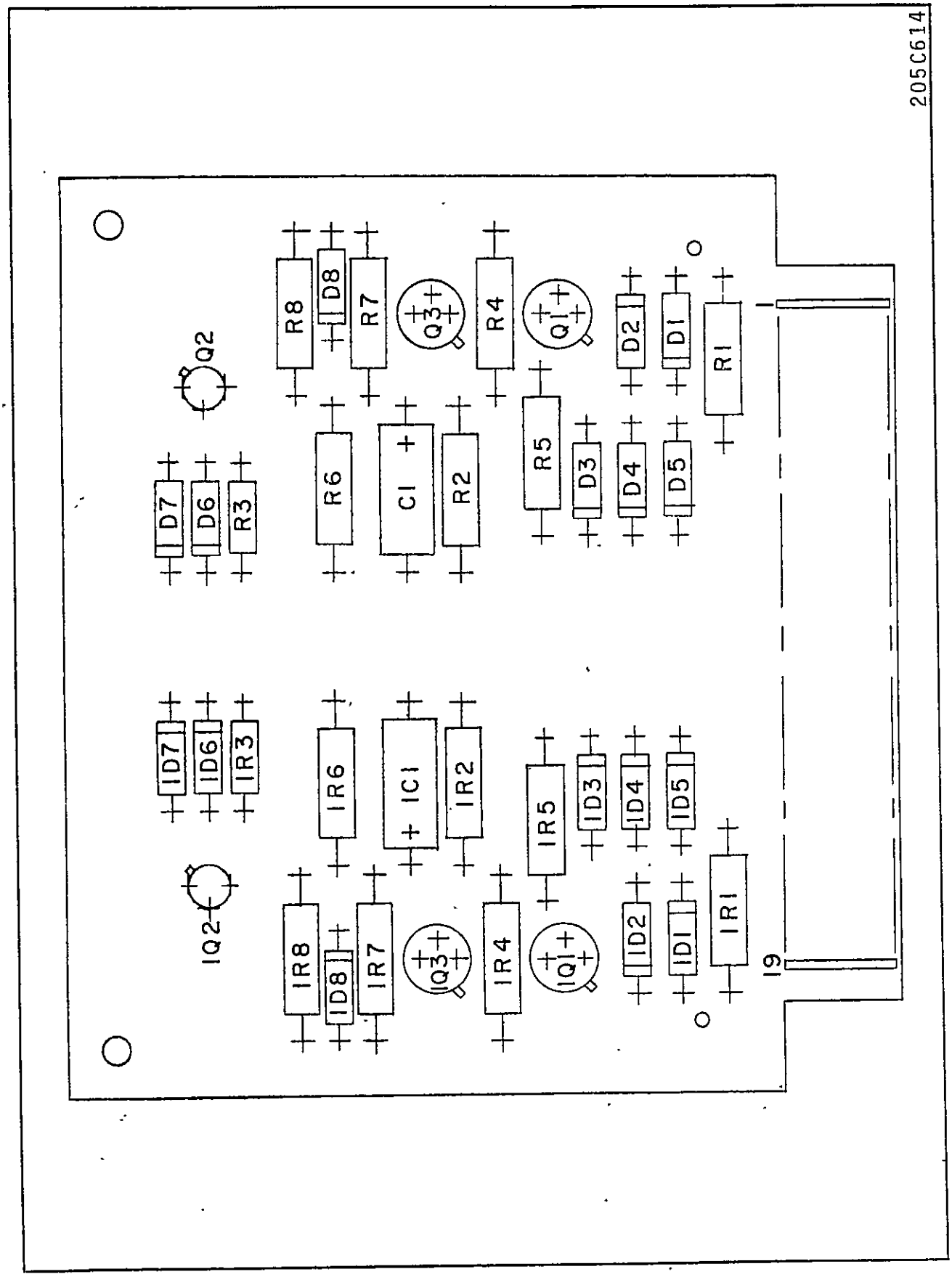


Fig. 10 Component Location Timers

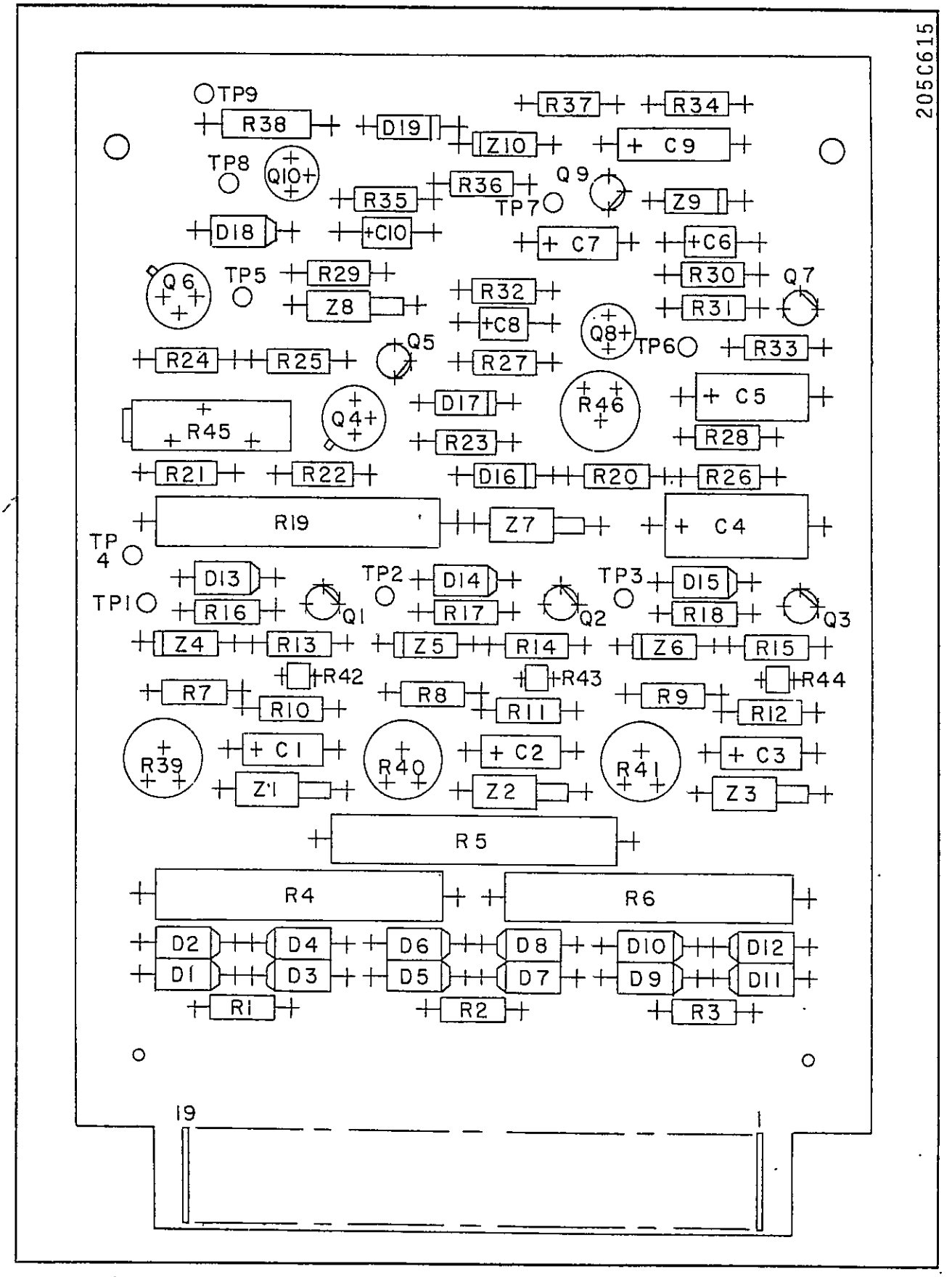


Fig. 11 Component Location Logic

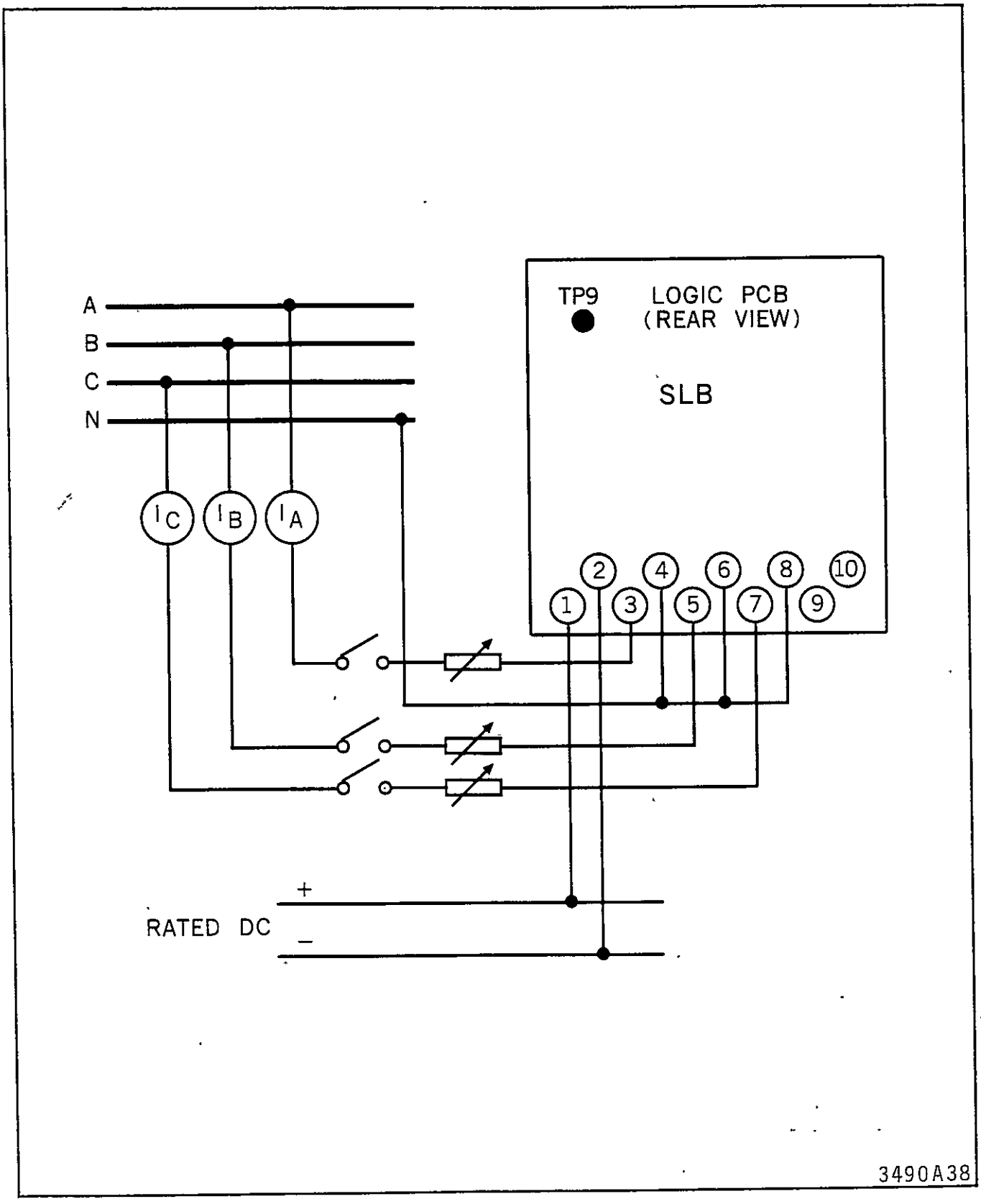


Fig. 12 Relay Test Figure